Since the waveforms developed by the twelfth counter are used for several applications, the outputs of the twelfth counter are fed to the grids of cathode followers in order that the twelfth counter is not loaded heavily by these external circuits. Figure 12 shows the cathode follower tube, V125 and indicates the circuits which use the twelfth counter waveforms supplied by the cathodes of V125. The output of cathode follower, V125A, is fed to:

(1) The twelfth counter amplifier, V127A, which develops the trace separation voltage which is applied to the vertical plates of the CRT.

(2) The amplitude balance circuit (V126) which provides an independent gain control of the receiver top trace with respect to the bottom trace.

(3) The third delay coincidence amplifier, V119B, which gates the variable delay (slave) pedestal so that it occurs only during bottom trace time.

The output from Section B of V125 is fed to:

(1) The master pedestal delay gate tube, V146, where it is used to develop the master pedestal trigger.

(2) The amplitude balance circuit.

The various circuits using these waveforms will be described in succeeding sections.

TION 1 TRACE SEPARATION CIRCUIT

Since the twelfth counter is not controlled by the reset pulse, the output of the left plate could produce either a positive or negative wave when the first reset trigger (shown in Line B of Figure 12) arrives. It really doesn't matter which is produced first, since a positive waveform from pin 3 of V125A will always produce the master trace, and a negative waveform will always produce the slave portion of the sweep. This can be seen with the help of Figure 12 and the complete Indicator schematic, Drawing J126. Suppose the output of cathode follower, V125A is as shown on Line C; that is, a positive wave of 15,000 microseconds duration followed by a negative wave of 15,000 microseconds duration, etc. This waveform is fed to V127A which amplifies and inverts this waveform. Thus, the positive portion has become negative and the negative portion positive. This inverted output from the plate of V127A is fed directly to the <u>bottom</u> vertical plate of the cathode ray tube. Making this plate more negative results in the beam being deflected <u>upward</u> and this produces the top, or master trace. When the positive waveform appears, the beam is deflected <u>toward</u> the plate (downward) to produce the bottom, or slave trace.

17.13 MASTER PEDESTAL TRIGGER

As described earlier, the master pedestal is stationary and is displaced from the left side, or start, of the top sweep a fixed amount for convenience in viewing. Since the top sweep is started by a reset pulse, the master pedestal trigger is delayed from this point 1600 microseconds by combining outputs from the 8th and 12th counters in a manner which can be understood with the aid of Figure 13.

The output of the right plate of the 8th counter is shown in Line B of Figure 13. This output consists of negative and positive square waves, each 1600 microseconds wide. At reset, of course, the right plate is mad to conduct and, therefore, the first 1/2 cycle of the waveform after rese will be negative for 1600 microseconds and then it will go positive for t next 1600 microseconds, etc. This output is fed to the grid of a cathode follower, V128A in order that this output may be used without undue loading of the 8th counter stage. This output appears on the cathode unchang but the square wave is differentiated by small capacitor C160 and resist R238 to produce the series of pips shown in Line C. (A differentiating circuit produces a sharp, positive pip when a square wave goes positive, and a sharp, negative pip when the square wave goes negative). Notice that the first positive differentiated pip comes 1600 microseconds after reset and succeeding positive pips come every 3200 microseconds later. These differentiated pips shown in Line C are fed to the second half of tube V128. This tube, V128B, is held very nearly at cut off by the lar self-bias developed by the cathode resistor, R240. It thereby acts as clipper tube and prevents the negative pips, applied to the grid, from being amplified. The positive pips applied to the grid, however, are a fied and inverted to form a series of negative pulses on the plate of t tube. These are shown in Line D. From here, they are coupled to the of the master pedestal delay gate, V146B.

The output from the twelfth counter cathode follower, V125B (Line D of Figure 12) is also shown as Line E of Figure 13. This waveform, negative wave 15,000 microseconds long, followed by a positive sectio equal length, is fed to the grid of the master pedestal delay gate, a verted to produce the waveform shown on Line F of Figure 13. This wa form is differentiated by C156 and R229 to form the waveform shown on G. This output is then coupled through R230 to the grid of V146B wh combines with the pips from V128 (Line D) to produce the resulting w form shown on Line H.

Now the grid of V146B is returned to minus 105 volts through R2 Therefore, this section of the tube is biased to cut off and will c only when the input signal (Line H) is most positive. This tube ac as a clipper and all negative portions of the input wave are clippe resultant output is shown as Line I of Figure 13. Only the positiv tions of input signal (Line H) have been passed and inverted.

This plate output, Line I, is coupled to the grid of the pede erator through a differentiating circuit, C203 and R361, which pro trigger shown in Line J. This positive trigger, which occurs 1600 conds from the master reset pulse, is used to trigger the pedestal to form the master pedestal.

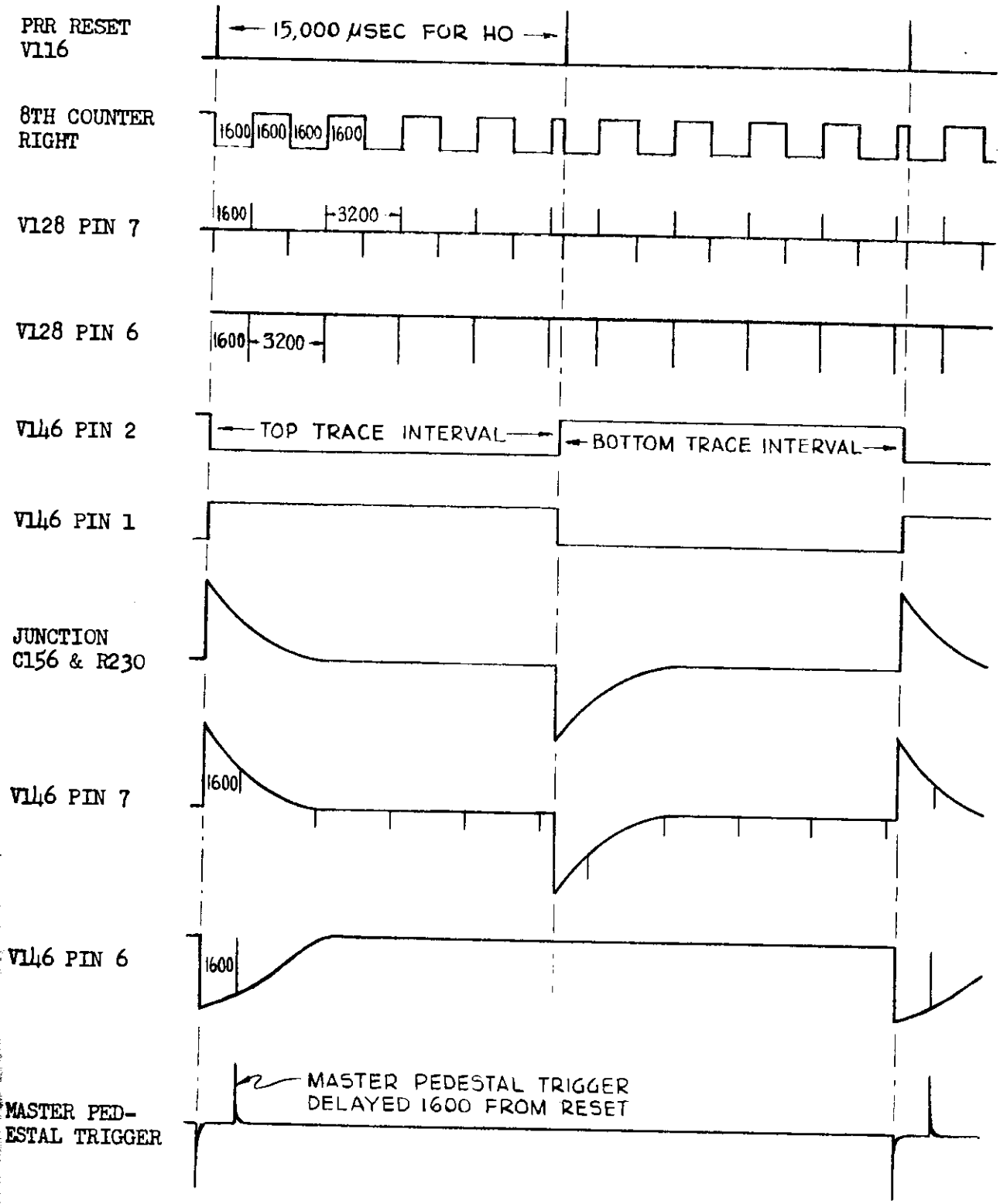


Figure 13
GENERATION OF MASTER PEDESTAL TRIGGER

Notice that no trigger is developed during the period following the reset pulse which generates the slave sweep since the waveform on the grid of V146B is extremely negative at this time and V146B can only conduct for positive portions of the input signals.

17.14 PEDESTAL GENERATOR

The generation of a master pedestal trigger delayed 1600 microseconds from the master reset trigger has been described, and in a later section the development of a trigger by the delay circuits will be discussed. Both these triggers are fed to the pedestal generator, V143, which develops from these triggers the master and slave pedestals.

The pedestal generator tube, V143, is a standard one-shot, cathode-coupled multivibrator circuit. This means that the multivibrator will make one complete cycle, or flip-flop, for each input trigger.

Section A of tube V143 is normally cut off because section B is conducting heavily (grid returns to +B through R366) and develops enough cathode bias across R364, the common cathode resistor, to keep section A cut off. However, when a positive input trigger appears at the grid of section A, this section will conduct. The resultant drop in plate voltage of section A is then coupled through C204 to the grid of section B which tends to make section B conduct less. This, in turn, causes less cathode bias to be developed across the common cathode resistor, thus causing A to conduct still more heavily. This effect is cumulative and almost instantaneous, and soon the A section is conducting heavily and B section is cut off.

Section B will remain cut off until C204 recharges through R366 and R392 to +B. As soon as C204 becomes positive enough to overcome the bias produced by the drop in plate voltage of A, section B will conduct again, and in doing so, will cut off section A and both sections will remain in this state until another positive trigger arrives at the grid of section A. Thus, the tube has made one complete cycle, and a voltage waveform is produced on each plate of the pedestal generator tube. The width of pedestal (i.e., the time section A conducts or the time section B is cut off) can be varied from approximately 800 to 1600 microseconds by adjusting R362, the PEDESTAL WIDTH potentiometer. Changing this control affects the amount of plate current drawn by section A. This, in turn, changes the cathode current which affects the cut off time of the B section.

In FUNCTION 3 the pedestal generator does not need to be very wide. Therefore, the grid return resistance for the B section is reduced by shorting out R392 by contacts 11 and 12 of S102C. Thus, the B section will start conducting approximately 200-250 microseconds after section A has been triggering.

The pedestal generator output is fed to:

(1) Pedestal amplifier, V127B, and then to vertical plates of CRT.

(2) Sweep generator tube for FUNCTION 2 and 3 sweep.

(3) A.F.C. circuit where it is used as a gate.

Notice that the output of the pedestal amplifier tube, V127B, is mixed across R374 with the output of the twelfth counter amplifier, V127A. This common point is isolated from the pedestal amplifier by R372 and from V127A by R234. This mixed output is then fed to the vertical plates of the cathode ray tube.

In FUNCTION 2 the pedestal amplifier output is removed from the mixing network and the output of the twelfth counter amplifier, V127A, establishes the vertical deflection between the two CRT traces during the sweep time.

.15 AMPLITUDE BALANCE

The amplitude balance and gain control circuit is unique in that although both these controls are direct coupled to the receiver by means of the same wire, independent operation of either circuit is possible. This circuit will be explained with the aid of Figure 14.

Both plates of tube V126 are returned to ground and the cathodes are tied to -105 volts through a common cathode resistor. Thus all voltages in this circuit are negative with respect to ground.

On each grid of the amplitude balance tube there is applied a square wave from the twelfth counter cathode follower, V125. The grid of section A (pin 2) receives the waveform shown in Line A of Figure 14, and the grid of section B (pin 7) receives the waveform shown on Line B. Notice that these waveforms are 180 degrees out of phase; i.e., when A is positive, B is negative.

Three conditions of operation will now be discussed to illustrate the action of this circuit. They are:

(1) Balance control centered. (Both traces have same sensitivity.)

(2) Balance control completely counterclockwise (top trace less sensitive than bottom trace).

(3) Balance control completely clockwise (top trace more sensitive than bottom trace).

(1) Balance control centered. In this case, the arm of the balance control is connected to the top of the gain potentiometer through the center tap on the balance potentiometer. For such a setting, each triode has exactly the same plate load resistance. With no inputs to the grids of these two sections, self bias is developed across the common cathode resistor, R220, which biases each section to approximately cut off. When the square waves shown on Lines A and B are applied to the grids, plate current will flow only during the time the wave is positive, since only then will the bias, developed across R220, be overcome. Since the grid inputs are 180 degrees out of phase, sections A and B of the tube will conduct alternately, and because both sections of the tube are symmetrical, a steady current

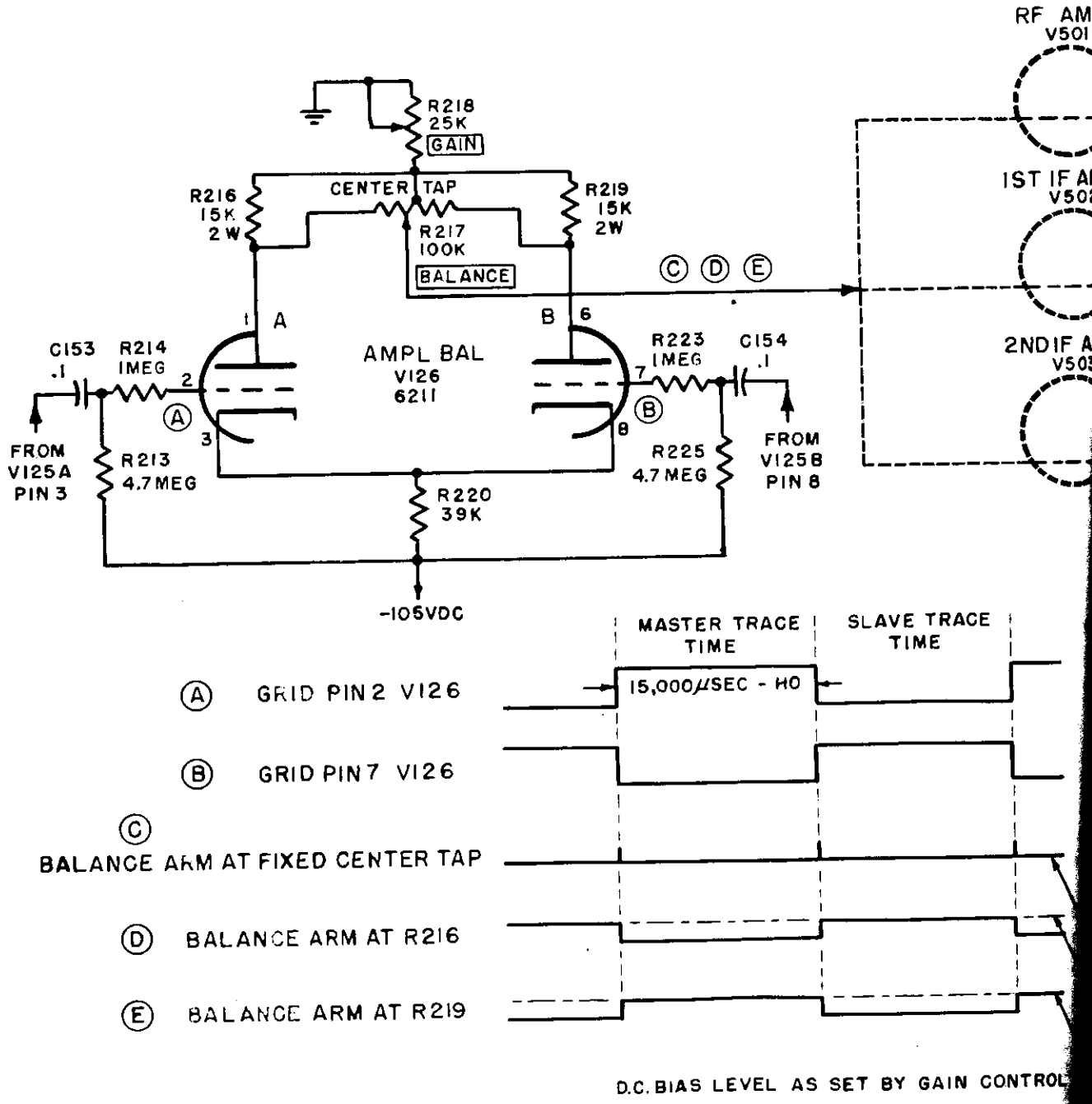


Figure 14

SIMPLIFIED AMPLITUDE BALANCE CIRCUIT

will flow through the common cathode and common plate resistor (gain control) of the tubes. Thus, the voltage drop across resistor, R218, is constant, and with the balance control in this center position, the output to the receiver tubes is a DC voltage, the value of which depends on the setting of the gain control, R218. The sensitivity of each trace is the same and is adjusted by the gain control setting.

(2) Balance control counterclockwise. In this case, the arm of the balance control is connected to the plate of section A. During the time the input waveform to the grid is negative, section A is cut off and no voltage is developed across the plate resistor, R216. Therefore, the voltage on the plate (and hence, on the balance potentiometer arm) is that established by the voltage across the gain control (developed by the current thru B section during this time). However, during the time the grid of section A is positive, the tube conducts and a voltage drop is developed across R216. This drop is added to the voltage established by the drop across the GAIN potentiometer. It should be realized, however, that both sections of the tube, due to the alternate positive waves on the grids, are still producing an effective DC voltage to be developed across the gain resistor as described in the preceding paragraphs.

(3) Balance control clockwise. In this case, the balance arm is on the plate of section B, and the output is shown on Line E of Figure 14. The action in this case is exactly opposite to that described in the preceding paragraph; that is, during master trace time the bias fed to the receiver is clamped at the setting of the gain control (since plate of section B is cut off) and during the slave trace time the plate of section B conducts and the sensitivity of the receiver is reduced.

16 MANUAL AND AUTOMATIC FREQUENCY CONTROL

As previously explained, the repetition rate accuracy of the various sweep outputs is determined by the 80 kc crystal controlled oscillator, V102A. When the repetition rate of the LR-8803 sweep is exactly equal to the repetition rate of the desired Loran signals, the signals and sweeps will be synchronism, and the signals will be stationary on the screen. However, it is impossible to expect the LR-8803 crystal to be exactly the value to give us perfect synchronism with the received signals (due to tolerances on the receiver crystal as well as transmitter tolerances) and therefore, signals to which the Loran set is switched, might drift very slowly across the screen. To allow the operator to readjust the Loran crystal oscillator to correct for these slight differences in frequency, two means of frequency control are provided in the Loran indicator. They are:

a) Manual control of frequency (DRIFT).

b) Automatic frequency control (AFC).

In either case, DRIFT or AFC operation, changes of the crystal oscillator are affected by the action of the reactance tube circuit, V101, and this circuit will now be described.

It is a well-known fact that the frequency of a crystal can be changed a small amount by varying the capacity shunted across it. In the LR-8803 crystal oscillator circuit, the crystal is effectively shunted by a reactance tube, V101, which tends to change the resonant frequency of the crystal in the following manner. Since the reactance tube is connected across the crystal, the oscillator grid signal voltage thereby appears on the reactance tube plate. This plate voltage signal is fed back to the grid of the reactance tube by a phase shift network consisting of C103 and R102. The network shifts the phase of the 80 kc signal in such a manner that the signal voltage on the grid is almost 90 degrees ahead of the plate signal. Thus, the grid signal causes current changes in the reactance tube which will lead the plate voltage by almost 90 degrees. This means, in effect, that the tube is acting like a capacitor (i.e., the current through the tube leads the voltage across the tube). By varying the gain of the reactance tube the effective capacity in the plate circuit can also be changed. This capacity change across the crystal will change the oscillator frequency as indicated in the chart below.

DC Grid Voltage Tube V101	DC Reactance Tube Current	Capacity across Crystal	Crystal Frequency
more negative	decreases	decreases	increases
less negative	increases	increases	decreases

In the DRIFT position, the frequency of the oscillator is decreased or increased by moving the DRIFT knob counterclockwise or clockwise, respectively.

Once signals have been properly positioned on top of the pedestals, the AFC circuit can be used to keep the signal stationary. Its operation will be described with the aid of Figure 15. It consists basically of a discriminator circuit where the pulse repetition rate of the signal is compared with the sweep rate generated in the Loran indicator. Any difference between these rates results in a corrective voltage which is fed to the reactance tube grid in such a manner as to cause the crystal oscillator frequency (and hence, sweep rate) to equal the PRR of the received signal.

Line A of Figure 15 shows the PRR reset pulses for the HO rate. Line B shows the master and slave pedestals, and in Line C the time scale is expanded to show the shape of the master and slave pedestals.

From the pedestal generator, V143, the positive gate is fed to the differentiating circuit consisting of C162 and R241 which produces the output shown in Line D. This differentiated output appears on the grid of the "A" multivibrator, V129. This tube is a "one-shot" multivibrator, and goes through one single cycle when triggered by a positive input pulse. (Notice similarity to pedestal generator.) The output pulse (pin 6) is 75 microseconds long, and is shown on Line E. Notice that the 75 microseconds out from the "A" multivibrator is much narrower than the 1200-1600 microsecond pedestal generator output. In addition, a pulse of opposite polarity appears on the other plate of the multivibrator, pin 1, and this is shown on Line F. When this output is differentiated (by C163 and R244) a positive trigger will be formed at the trailing edge of the "A" multivibrator output gate (Line E). This positive trigger causes the "B" multivibrator, V130, to complete a cycle producing the output shown in Line H.

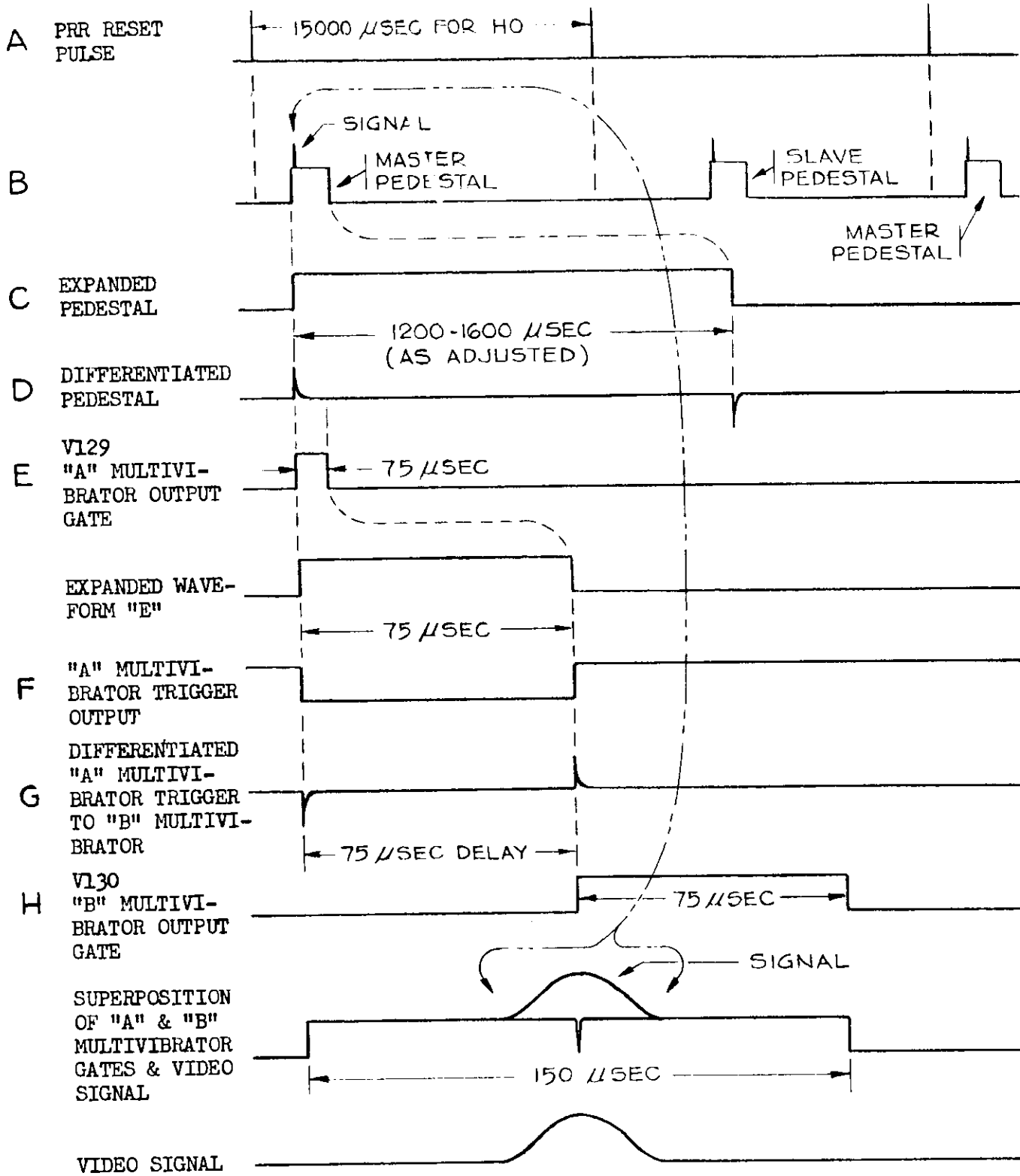


Figure 15

AFC WAVEFORMS

To summarize the action described previously:- The differentiated leading edge of either the master or slave pedestal is used to trigger the "A" multivibrator which produces a positive gate 75 microseconds long. At the end of the "A" multivibrator gate, a "B" multivibrator gate is started which also lasts for 75 microseconds.

(Bear in mind the total duration of the "A" and "B" multivibrator gates are equal to 150 microseconds. Since the pedestals are 1200-1600 microseconds wide, AFC will only operate properly when the signals are positioned near the left 10% of the pedestals (the first 150 microseconds).)

Now consider what happens if the outputs of the "A" and "B" multivibrators are used as gates for the received video signal. Negative video signals from the receiver are inverted by the video amplifier, V131A, and appear as positive signals on the plate of this tube. This signal is applied to the grids of the "A" and "B" gate amplifiers, V133 and V132. The output of the "A" multivibrator is applied to the suppressor of V133 and the output of the "B" multivibrator is applied to the suppressor of V132. Plate output due to the input video signals applied to the grids will only be present when the "A" and "B" multivibrator outputs are supplied to the suppressors.

Now assume that a signal appears on the grids of V133 and V132 during the time of the "A" multivibrator output only. Then a negative pulse appears at the plate of V133. This pulse is fed to the "A" limiter, V134A, which is a cathode follower. This tube limits the amplitude of the output signal, but does not change its polarity. Thus, the negative output on the cathode of V134A is fed to the input of the "A" discriminator, V135A. This causes the capacitor, C174, in the plate output to charge and develop a negative voltage across R277. Since the video pulse appears on the "B" gate amplifier grid during the time there is no "B" multivibrator gate, there is no plate output from tube V132, and hence, the "B" limiter produces no output to be supplied to the "B" discriminator, V135B. The net result, then, is a negative output of the discriminator across R277 due to the "A" channel. This negative voltage (in AFC) is applied to the reactance tube grid which causes the frequency of the crystal to increase which, in turn, causes the signals on the screen to move to the right (and, therefore, toward the "B" multivibrator gate).

Now if a signal appears during the time of "B" multivibrator output, a negative plate output appears at the plate of V132. This is inverted and limited by the "B" limiter, V134B. The positive output from V134B is fed to the plate of the "B" discriminator, V135B, which causes a less negative voltage to appear across R277. (Less negative because the other end of R277 is connected to a negative bias.) The "less negative" voltage, when applied to the reactance tube grid, causes more capacitive loading across the crystal, and hence, a lower crystal frequency which moves signal to the left (and, therefore, toward the "A" multivibrator gate).

If the action described above is understood, it must be apparent that if the video signal is centered between the end of the "A" multivibrator gate, and the beginning of the "B" multivibrator gate, equal and opposite voltages will be developed by the discriminators, which cancel, and the

reactance tube bias remains unchanged. However, an unbalance due to a change in the rate of the sweep or the signal, will cause a change of voltage of such magnitude as to cause the crystal to assume a new frequency which keeps the rates equal. Thus, the sweep and the signal are automatically locked at the same rate.

Notice that the AFC action occurs on both the master and slave signals. This results in AFC action that is twice as "smooth" as either alone since AFC correction occurs at twice the repetition rate. In operation the master signal is placed on the master pedestal and then the operator switches the DRIFT knob to AFC. With the master signal then "locked-in" the delay pedestal can be moved to a position under the slave signal.

Note, too, that the DRIFT control is used also in the AFC position. This allows the operator to position the signals on the FUNCTION 3 sweep when in AFC. It is also used to indicate whether the AFC is functioning properly, for in such a case the signals should remain "locked-in" over practically the full rotation of the DRIFT control. This is a good test of AFC operation since manually turning the DRIFT knob manually changes the bias on the reactance tube. To correct for this manual change of bias, the AFC circuits must work in such a manner as to always present the correct bias to keep the signals "locked-in". In AFC operation, the DRIFT control should be left centered in its range of control.

17 LEFT-RIGHT OPERATION

When a Loran receiver is switched to a particular station rate, the master and slave signals, which stop on the CRT, may stop anywhere on the trace. The operator must then move the signals along the trace until the master signal is atop the master pedestal. To allow him to do this quickly and conveniently, the LEFT-RIGHT switch is provided on the front panel to move the signals either left or right to the position desired.

This movement of the signals to the left or the right is accomplished by altering the period between reset pulses as tabulated below for the HO rate.

RATE HO

LEFT-RIGHT SWITCH	PERIOD BETWEEN RESET PULSES	
	FUNCTION 1	FUNCTION 2 & 3
LEFT	15,112.5	15,012.5
NORMAL	15,000	15,000
RIGHT	14,887.5	14,987.5

Notice that when the LEFT-RIGHT switch is in the LEFT position, the period between reset pulses is increased by 112.5 microseconds when in FUNCTION 1. Thus a definite difference in rates is created between indicator and received signals and they will drift to the left on the CRT screen.

Notice that for FUNCTION 2 and 3, the period is increased by only 12.5 microseconds. This is done so that for FUNCTION 2 and 3 the signals will drift across the screen at the same speed as they do on FUNCTION 1. (Remember that the CRT trace time on FUNCTION 2 is established by the pedestal width, approximately 1000 usec, and not the full Loran cycle.)

When in the RIGHT position, the Loran cycle is decreased by 112.5 usec in FUNCTION 1, and decreased by 12.5 in FUNCTION 2 and 3.

Circuit operation is as follows:- When in the RIGHT position, the reset pulse instead of being fed back to the right grids of the 1st and 4th counters (FUNCTION 1), is fed to the left grids of these tubes. In this fashion, the PRR coincidence interval is shortened by 112.5 usecs, the sum of $\frac{1}{2}$ periods of the 1st and 4th counters. When in FUNCTION 2 and 3, only the 1st counter is so affected, and the period is shortened by 12.5 usecs only.

When the switch is in the LEFT position, for each reset pulse, nine successive cycles of crystal oscillator pulses (12.5 microseconds each) are gated out for FUNCTION 1. For FUNCTION 2 and 3, only one 12.5 microsecond drive pulse is gated out. This is accomplished by feeding the negative pulse from the plate of the reset generator, V116, back to the grid of the ringer tube.

The pulse is fed back through C123, the LEFT switch, and C114 to the grid of the ringer, V102B. For FUNCTION 1, C123 acts with R120 to partially differentiate the pulse. For FUNCTION 2 and 3, R123 is placed across R120 and complete differentiation of the negative pulse takes place, resulting in a smaller negative pulse being fed back to the ringer tube.

17.18 DELAY CIRCUITS

The second important function of the Indicator is to provide a delay system which must be continuous, accurate and have a wide range (0 to greater than 10,000 microseconds).

The LR-8803 delay system uses combinations of waveforms obtained from the counter outputs to form a pulse which can be varied in time. This provides a coarse measure of delay time. The accuracy is obtained by using this coarse delay in conjunction with a 100 microsecond accurately phase-shifted pulse.

Coarse Delay Pulse

First let us review the waveforms obtained from the 3rd, 4th and 5th binary counter stages (tubes V106, V107 and V108). Outputs from both the left and right hand sections of the counters are shown in Figure 16. Now these 6 waveforms can be added together in all sorts of different combinations to produce a new waveform. This adding is done by choosing particular counter outputs by means of a switch and by combining them in gating circuits to produce the desired coarse delay output pulse.

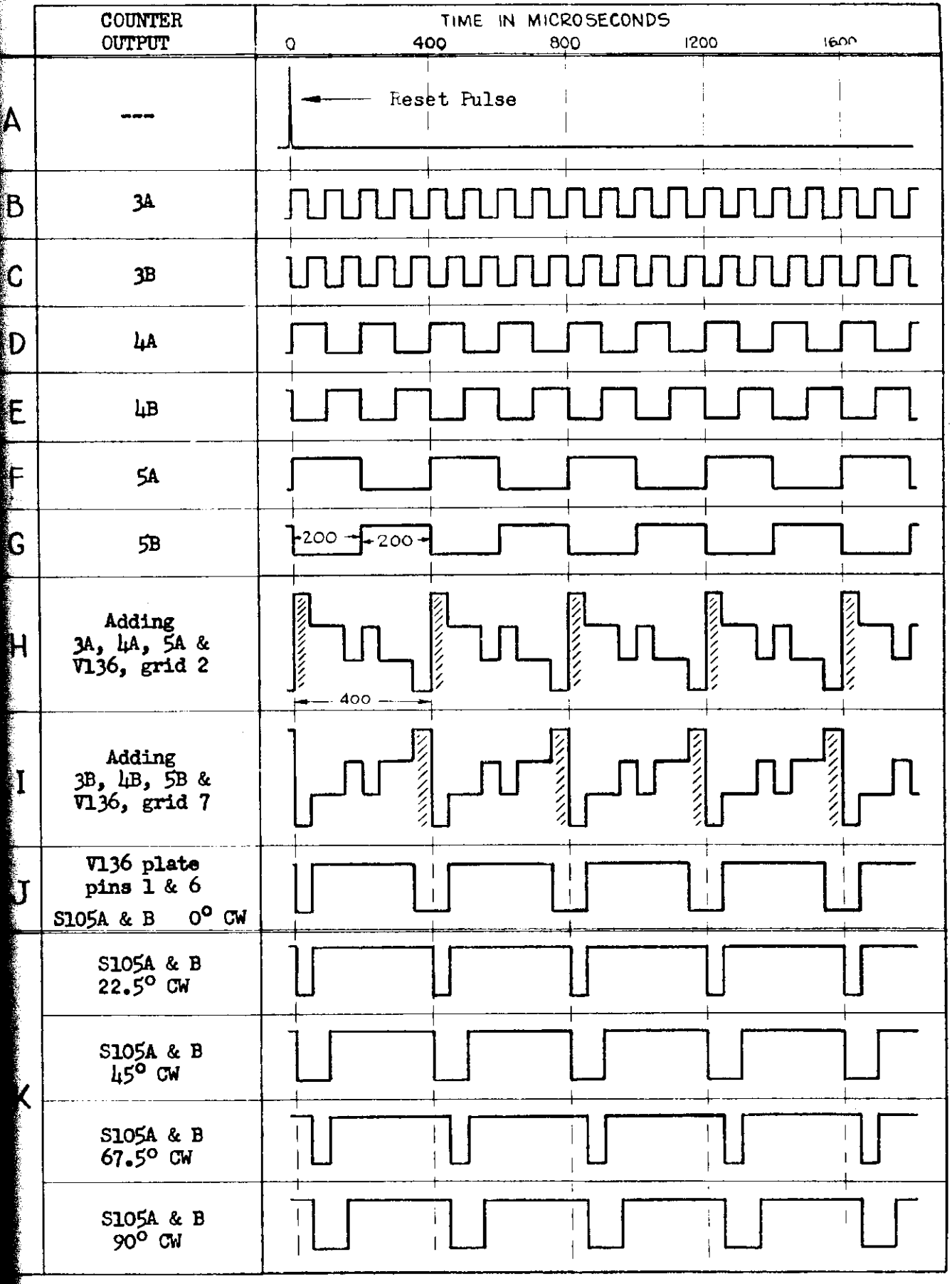


Figure 16

DELAY CIRCUIT COUNTER OUTPUT WAVEFORMS

Figure 17 shows the switches and gating tubes used with the 3rd, 4th and 5th counters. Note that the front and rear rotor sections of both wafer, S105A and wafer, S105B are electrically connected (soldered) together. This allows us to add three waveforms together on each of these two wafers, and when necessary, to disconnect this summed waveform by means of the switch.

Line H of Figure 16 shows the resultant waveform obtained when all left outputs of the 3rd, 4th and 5th counters are added. Line I shows the resultant waveforms obtained when all the right outputs of the 3rd, 4th and 5th counters are added. Figure 17 illustrates the simplified diagram showing the counter connections required to produce these waveforms.

Now consider what happens when these two waveforms from the switch outputs are added together. On pin 2 of V136, the 3A, 4A and 5A summed waveform is applied and on pin 7, the summed waveform of the 3B, 4B and 5B counters is applied. This gate tube, V136, is biased in such a manner that only during the time the waveform on either grid is at its maximum positive voltage will any output be produced in the plate circuit. If the waveforms on Figure 16, Lines H and I are introduced into the grids of V136, the resultant plate output is shown on Line J. Note that from reset (point 0) to point 1, there is an output 50 microseconds wide and that an output 100 microseconds wide will occur every 400 microseconds later until reset time is reached again. For the particular output shown on Line J, this pulse occurs between 350-450 microseconds, 750-850 microseconds, etc. Now assume this occurs when the switch S105 is set on a position which we call 0°. Now suppose we rotate the rotor of this switch. Until we reach the next position on the switch (which we will call 22.5° rotation), we will continue to get the waveform shown on Line J at the plate circuit of V136. However, when this next position is reached, a new group of waveforms is fed into the grids of V136 and a new output results on the plate. This new output will be a pulse only 50 microseconds wide occurring between the times 400-450 microseconds, 800-850 microseconds, etc. In this position, S105B disconnects the added waveform from 3B, 4B and 5B counters to grid 7, V136.

Now if switch S105 is rotated from 22.5° to 45°, the new output will remain for this interval, but when the 45° point is reached, new waveforms are switched into the grids of V106 and a new pulse is formed which starts at the same time as the preceding output (400 microseconds, 800 microseconds, etc.) but is now 100 microseconds wide. Note that the 50 microsecond gates are formed by removing one set of the pair of input signals to V136 which make up the 100 microsecond gate. The 45° position output is shown at K of Figure 16.

Thus, it is evident that as the rotor of switch S105 is turned, the plate output of V136 consists of alternate 50 and 100 microsecond pulses (negative) which continually move to the right. Every 400 microseconds the cycle is repeated. V136 is called the 50-100 microsecond delay gate because its output consists of a negative gate which is successively 50 and 100 microseconds in width. Note that this cycle repeats itself at intervals of 400 microseconds. Thus, the same output of V136 occurs at 320 microseconds, 720 microseconds, 1120 microseconds, etc. Figure 18 shows the output waveforms of the 50-100 microsecond delay gate for various positions of the DELAY switch, together with a list of the various counter

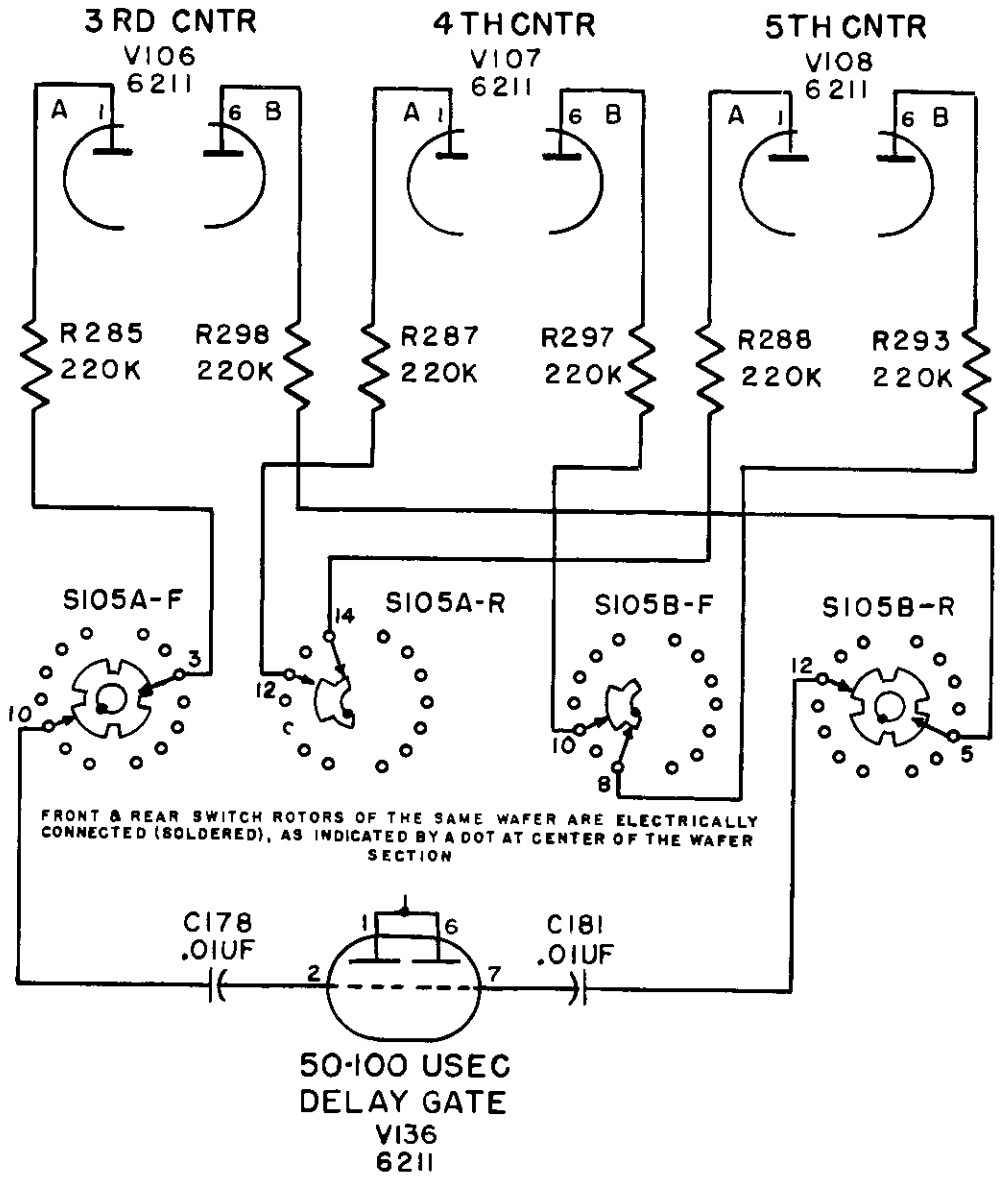
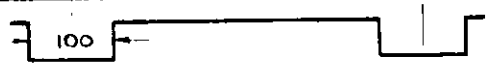
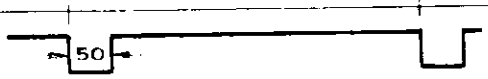
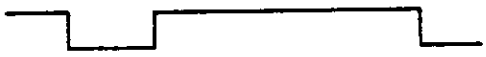
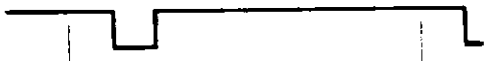
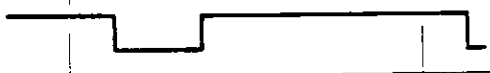
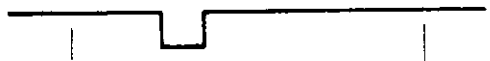
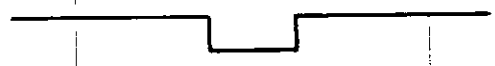
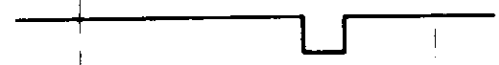
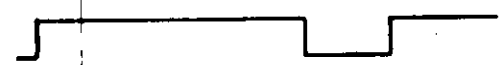
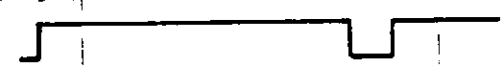
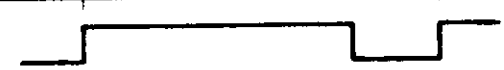
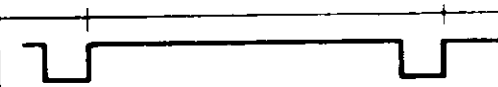
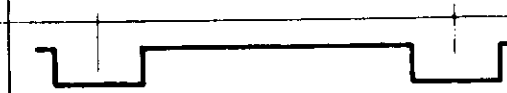


Figure 17

SIMPLIFIED CONNECTIONS TO V136

	TIME DIFFERENCE READING	POSITION OF S105A&B (DEGS. CW)	400 MICROSECONDS ONE WAVEFORM CYCLE	GRID SIGNALS = SUM OF	
				V136 PIN 2	V136 PIN 7
A	01587	0°		3A,4A,5A	3B,4B,5B
B	01612	22.5°		3A,4A,5A	SWITCH OPEN
C	01637	45°		3A,4A,5A	3B,4A,5A
D	01662	67.5°		SWITCH OPEN	3B,4A,5A
E	01687	90°		3A,4B,5A	3B,4A,5A
F	01712	112.5°		3A,4B,5A	SWITCH OPEN
G	01737	135°		3A,4B,5A	3B,4B,5A
H	01762	157.5°		SWITCH OPEN	3B,4B,5A
I	01787	180°		3A,4A,5B	3B,4B,5A
J	01812	202.5°		3A,4A,5B	SWITCH OPEN
K	01837	225°		3A,4A,5B	3B,4A,5B
L	01862	247.5°		SWITCH OPEN	3A,4A,5B
M	01887	270°		3A,4B,5B	3A,4A,5B
N	01912	292.5°		3A,4B,5B	SWITCH OPEN
O	01937	315°		3A,4B,5B	3B,4B,5B
P	01962	337.5°		SWITCH OPEN	3B,4B,5B
Q	01987	360° or 0°		3A,4A,5A	3B,4B,5B

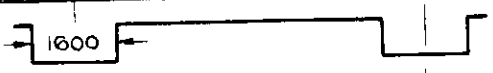
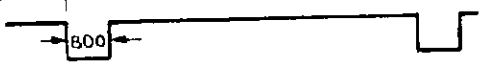
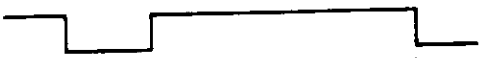
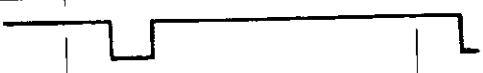
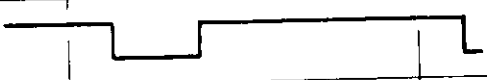
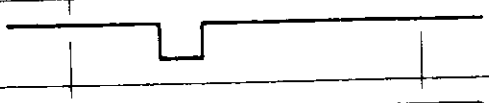
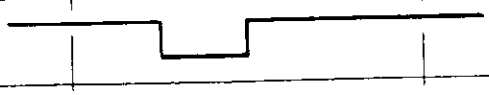
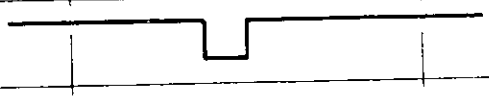
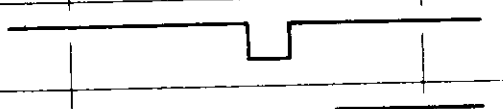
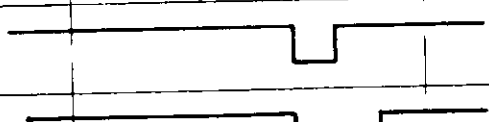
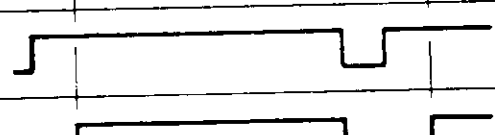
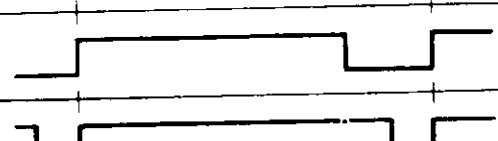
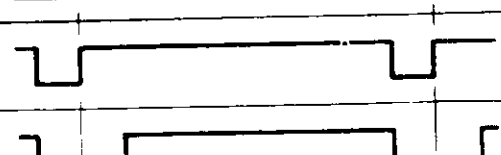
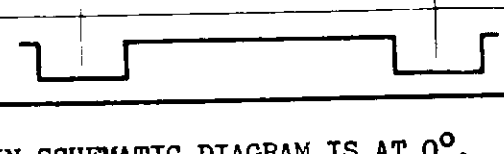
NOTES:
1. DELAY SWITCH AS SHOWN IN SCHEMATIC DIAGRAM IS AT 0°.
2. WAVEFORM SHOWN IS OUTPUT OF V136, PINS 1 AND 6. THIS WAVEFORM REPEATS ITSELF EVERY 400 MICROSECONDS (e.g.: WAVEFORM B OCCURS AT 00812,01212,01612).
3. 3A, 4B, ETC. REFER TO COUNTER STAGES, LEFT OR RIGHT PLATE AS SHOWN ON SCHEMATIC. (e.g.: 3A MEANS THIRD COUNTER, LEFT PLATE.)

Figure 18 OUTPUT WAVEFORMS OF 50 - 100 μSEC DELAY GATE

	TIME DIFFERENCE READING	POSITION OF S105C&D (DEGS. CW)	1600 MICROSECONDS ONE WAVEFORM CYCLE	GRID SIGNALS = SUM OF	
				V138 PIN 2	V138 PIN 7
A	01587	0°	400	5A,6A,7A	5B,6B,7B
B	01687	22.5°	200	5A,6A,7A	SWITCH OPEN
C	01787	45°		5A,6A,7A	5B,6A,7A
D	01887	67.5°		SWITCH OPEN	5B,6A,7A
E	01987	90°		5A,6B,7A	5B,6A,7A
F	02087	112.5°		5A,6B,7A	SWITCH OPEN
G	02187	135°		5A,6B,7A	5B,6B,7A
H	02287	157.5°		SWITCH OPEN	5B,6B,7A
I	02387	180°		5A,6A,7B	5B,6B,7A
J	02487	202.5°		5A,6A,7B	SWITCH OPEN
K	02587	225°		5A,6A,7B	5B,6A,7B
L	02687	247.5°		SWITCH OPEN	5B,6A,7B
M	02787	270°		5A,6B,7B	5B,6A,7B
N	02887	292.5°		5A,6B,7B	SWITCH OPEN
O	02987	315°		5A,6B,7B	5B,6B,7B
P	03087	337.5°		SWITCH OPEN	5B,6B,7B
A	03187	360° or 0°		5A,6A,7A	5B,6B,7B

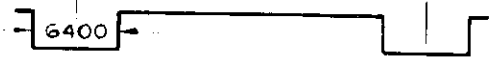
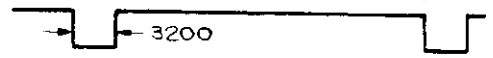
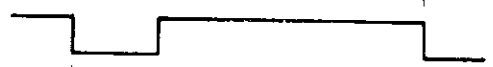
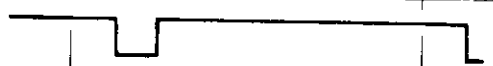
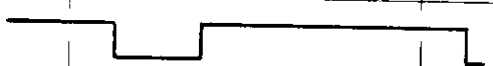
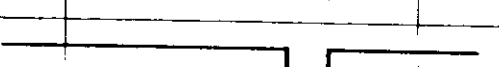
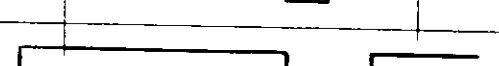
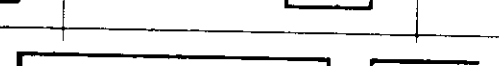
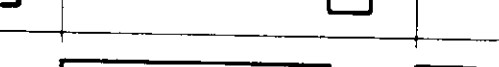
Y SWITCH AS SHOWN IN SCHEMATIC DIAGRAM IS AT 0°.
FORM SHOWN IS OUTPUT OF V138, PINS 1 AND 6. THIS WAVEFORM REPEATS IT-
EVERY 1600 MICROSECONDS (e.g.: WAVEFORM B OCCURS AT 99987, 01612, 03212).
4B, ETC. REFER TO COUNTER STAGES, LEFT OR RIGHT PLATE AS SHOWN ON SCHE-
C. (e.g.: 3A MEANS THIRD COUNTER, LEFT PLATE.)

19. OUTPUT WAVEFORMS OF 200-400 μSEC DELAY GATE

	TIME DIFFERENCE READING	POSITION OF S105E&F (DEGS. CW)	6400 MICROSECONDS ONE WAVEFORM CYCLE	GRID SIGNALS = SUM OF V139 PIN 2	V139 PIN 7
A	04787	0°		7A,8A,9A	7B,8B,9B
B	05187	22.5°		7A,8A,9A	SWITCH OPEN
C	05587	45°		7A,8A,9A	7B,8A,9A
D	05987	67.5°		SWITCH OPEN	7B,8A,9A
E	06387	90°		7A,8B,9A	7B,8A,9
F	06787	112.5°		7A,8B,9A	SWITCH OPEN
G	07187	135°		7A,8B,9A	7B,8B,9
H	07587	157.5°		SWITCH OPEN	7B,8B,9
I	07987	180°		7A,8A,9B	7B,8B,9
J	08387	202.5°		7A,8A,9B	SWITCH OPEN
K	08787	225°		7A,8A,9B	7B,8A,9
L	09187	247.5°		SWITCH OPEN	7B,8A,9
M	09587	270°		7A,8B,9B	7B,8A,9
N	09987	292.5°		7A,8B,9B	SWITCH OPEN
O	10387	315°		7A,8B,9B	7B,8B,9
P	10787	337.5°		SWITCH OPEN	7B,8B,9
Q	11187	360° or 0°		7A,8A,9A	7B,8B,9

NOTES:
1. DELAY SWITCH AS SHOWN IN SCHEMATIC DIAGRAM IS AT 0°.
2. WAVEFORM SHOWN IS OUTPUT OF V139, PINS 1 AND 6. THIS WAVEFORM REPEATS ITSELF EVERY 6400 MICROSECONDS (e.g.: WAVEFORM B OCCURS AT 98387,04787,11187
3. 3A, 4B, ETC. REFER TO COUNTER STAGES, LEFT OR RIGHT PLATE AS SHOWN ON SCHEMATIC. (e.g.: 3A MEANS THIRD COUNTER, LEFT PLATE.)

Figure 20. OUTPUT WAVEFORMS OF 800-1600 μSEC DELAY GATE

	TIME DIFFERENCE READING	POSITION OF S105G&H (DEGS. CW)	25,600 MICROSECONDS ONE WAVEFORM CYCLE	GRID SIGNALS = SUM OF V141 PIN 2	GRID SIGNALS = SUM OF V141 PIN 7
A	98387	0°		9A,10A,11A	9B,10B,11B
B	99987	22.5°		9A,10A,11A	SWITCH OPEN
C	01587	45°		9A,10A,11A	9B,10A,11A
D	03187	67.5°		SWITCH OPEN	9B,10A,11A
E	04787	90°		9A,10B,11A	9B,10A,11A
F	06387	112.5°		9A,10B,11A	SWITCH OPEN
G	07987	135°		9A,10B,11A	9B,10B,11A
H	09587	157.5°		SWITCH OPEN	9B,10B,11A
I	11187	180°		9A,10A,11B	9B,10B,11A
J	12787	202.5°		9A,10A,11B	SWITCH OPEN
K	14387	225°		9A,10A,11B	9B,10A,11B
L	15987	247.5°		SWITCH OPEN	9B,10A,11B
M	17587	270°		9A,10B,11B	9B,10A,11B
N	19187	292.5°		9A,10B,11B	SWITCH OPEN
O	20787	315°		9A,10B,11B	9B,10B,11B
P	22387	337.5°		SWITCH OPEN	9B,10B,11B
Q	23387	360° or 0°		9A,10A,11A	9B,10B,11B

NOTES:
1. DELAY SWITCH AS SHOWN IN SCHEMATIC DIAGRAM IS AT 0°.
2. WAVEFORM SHOWN IS OUTPUT OF V141, PINS 1 AND 6. THIS WAVEFORM REPEATS ITSELF EVERY 25,600 MICROSECONDS.
3. 3A, 4B, ETC. REFER TO COUNTER STAGES, LEFT OR RIGHT PLATE AS SHOWN ON SCHEMATIC. (e.g.: 3A MEANS THIRD COUNTER, LEFT PLATE.)

Figure 21. OUTPUT WAVEFORMS OF 3200-6400 μSEC DELAY GATE

outputs which are used as input signals for the grids of the delay gate. Notice on Figure 18 that there are 16 different waveforms. As the DELAY crank is turned through 400 microseconds, a new waveform is obtained every 25 microseconds with the result that the output continuously moves to the right. After 400 microseconds rotation, the cycle repeats.

In a similar manner, the outputs of the 5th, 6th and 7th counters are combined by switches S105C and S105D, and fed to the two grids of the 200-400 microsecond delay gate, V138. The output obtained on the plates of this tube is exactly similar in shape and behavior to those previously described, except now the waveform period is 1600 microseconds (corresponding to the period of the 7th counter) and the output pulse is successively 200 and 400 microseconds wide (as established by the 5th counter). Figure 19 shows the output waveforms versus switch position for the 200-400 microsecond delay gate.

Likewise the 7th, 8th and 9th counter outputs produce the plate waveform of the 800-1600 microsecond delay gate, V139. Here the waveform period is 6400 microseconds (as established by the period of the 9th counter) and the output waveform is successively 800 and 1600 microseconds in width (as established by the 7th counter). Waveforms for this delay gate output and grid connection are shown in Figure 20.

The same reasoning and waveforms hold true for the 3200-6400 microsecond delay gate, V141. Figure 21 shows the output waveforms and grid connections for this tube.

Now these various delay gate waveforms can be applied to coincidence tubes (similar to those used in the PRR section) in such a manner that either a 50 microsecond or 100 microsecond output will occur at one and only one particular time from reset time for a particular setting of the switches. Thus, as the switches are rotated, a continuous output pulse (which is successively 50 and 100 microseconds wide) can be formed. This is the coarse delay pulse. The manner in which this is done will now be described with the aid of Figure 22.

The top illustration of Figure 22 shows the four waveforms produced at the plates of the four delay gates when all switches are at an angle of 0°. This position of the switch occurs when the DELAY crank is rotated to the counter clockwise stop. This position corresponds to a time difference reading of 98387. There is only one point in time where all four waveforms go negative at once, and that is the time from reset to a point 50 microseconds from reset. Thus, these four waveforms are fed to the grids of the coincidence amplifiers, V137 and V140. As long as any section of these tubes is conducting, there is no output on the common plates, but if all four grids go negative at the same time (coincidentally) then and only then will there result a large positive pulse in the plate circuit. This output is shown in Line E. Notice that the coincidence output will only be as wide as the narrowest gate.

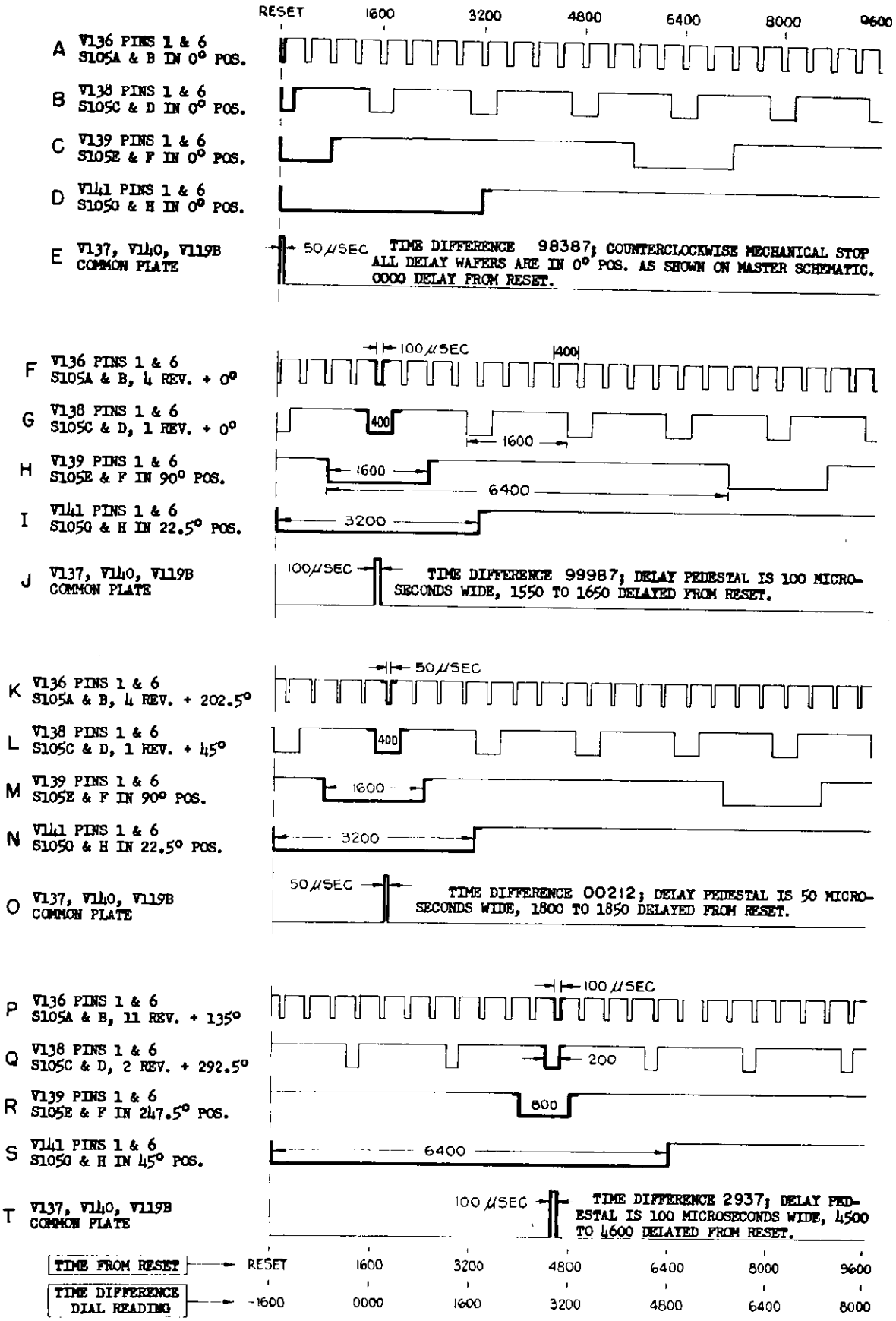
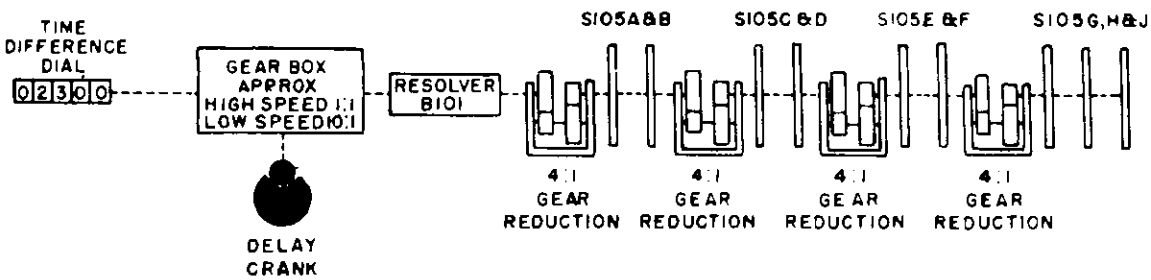


Figure 22

DELAY GATE OUTPUTS FOR VARIOUS TIME DIFFERENCES

As we have seen from the analysis of the 50-100 microsecond delay gate circuit, the waveform shown in Line A, Figure 18, will move continuously from reset to the end of its waveform cycle (400 microseconds), alternately forming 50 and 100 microsecond width gates. Thus, we can get a continuous output from reset to 400 microseconds by causing switch sections S105A and S105B to rotate one complete revolution. Switches S105C and S105D need not be rotated as much, however, because the gate width for this section is 200 or 400 microseconds and its period is 1600 microseconds. Also switch sections S105E and S105F need not be rotated as much as the previous sections because the waveform is negative for at least 800 microseconds and its period is 6400 microseconds. When sections S105A and S105B have made one complete revolution, sections S105C and S105D will have made a rotation of only 90°. Thus, it can be seen that sections S105C and S105D move only $\frac{1}{4}$ as much as the first sections S105A and S105B. This is accomplished by connecting the second set of switches to the first by means of gears in a 4:1 ratio. Similarly, the third set of switches need only rotate $\frac{1}{4}$ as fast as the second set and it, too, is geared to the second set through a gear mechanism of 4:1 ratio. The same reasoning applied to the fourth set of switches and it is likewise geared. Thus, every time the first set of switches is rotated 64 times, the second set revolves 16 times while the third set would make 4 complete revolutions and the last set only one. This arrangement results in a continuously variable coarse delay pulse from reset to a time over 10,000 microseconds away. Figure 23 tabulates the gear ratios between switch sections.



ONE COMPLETE REVOLUTION OF	RESULTS IN REVOLUTIONS OF				
	RESOLVER & TIME DIFFERENCE DIAL	S105A&B	S105C&D	S105E&F	S105G,H&J
TIME DIFFERENCE DIAL	1	1/4	1/16	1/64	1/256
S105A&B	4	1	1/4	1/16	1/64
S105C&D	16	4	1	1/4	1/16
S105E&F	64	16	4	1	1/4
S105G,H&J	256	64	16	4	1

Figure 23
GEAR REDUCTION RATIOS BETWEEN WAFERS

The remaining illustrations on Figure 22 show the various waveforms for various delay times from reset. Note that the TIME DIFFERENCE dial readings do not agree with the delay times as measured with the reset pulse. The reason for this difference will now be explained.

On FUNCTION 1, for ease of viewing, the master pedestal is delayed from the reset pulse (start of top trace) by 1600 microseconds. Therefore, in measuring the time difference between the delayed pedestal and the master pedestal, a fixed amount of 1600 microseconds must be subtracted from the distance of the delayed pedestal from reset in order for the dial to read correctly. Thus, the TIME DIFFERENCE, as read on the dial, will show a reading of 000 although this point is 1600 microseconds delayed from reset time.

Resolver Phase Shift Circuit

The positive 50 or 100 microsecond gate, as established by the delay coincidence amplifier, acts as the coarse selector for the delay pedestal. The accurate selection of time for the delay pedestal is generated by a continuously phase shifted pulse which rides atop the positive delay gate. Only a combination of delay gate and phase shifted pulse will produce a delay pedestal.

If we consider that a 50 microsecond delay gate has been obtained, then by phase shifting a pulse atop the gate, the output from the combination will move in time as the pulse moves atop the 50 microsecond gate.

Refer to Figure 24. The waveforms in A show the pulse near the left edge of the 50 microsecond delay gate. Then the delay trigger output (which is the combination of the resolver phase shifted pulse and the delay gate) is shown near the left edge of the gate. If the DELAY crank is rotated 25 microseconds the gate remains the same but the phase shifted pulse has moved to the right edge of the gate and the delay trigger occurs as shown in B.

If the DELAY crank is rotated further, the delay gate switches to a 100 microsecond gate (as previously explained). The phase shifted pulse moves further to the right and now occurs during the latter half of the 100 microsecond gate. The delay trigger is as shown at C.

Since the pulse is now riding atop the latter half of the delay gate, the front half of the gate is no longer needed and as the DELAY crank is further turned the front half of the gate drops out and a 50 microsecond delay gate is obtained. The phase shifted pulse is still atop the gate and the delay trigger is as shown at D.

Notice that the delay trigger always occurs directly under the phase shifted pulse, but only if there is a combination of positive phase shifted pulse and positive delay gate. It should be apparent that if the phase shifted pulse is smooth in its movement across the delay gate, the delay trigger will also be smooth in its movement. The purpose of the delay gate then, is to select one phase shifted pulse and exclude all others. The phase shifted pulse is a pulse which is derived from the third counter and, therefore, the period between any two positive phase shifted pulses is 100 microseconds. The pulse and its phase shifting is obtained in the following manner

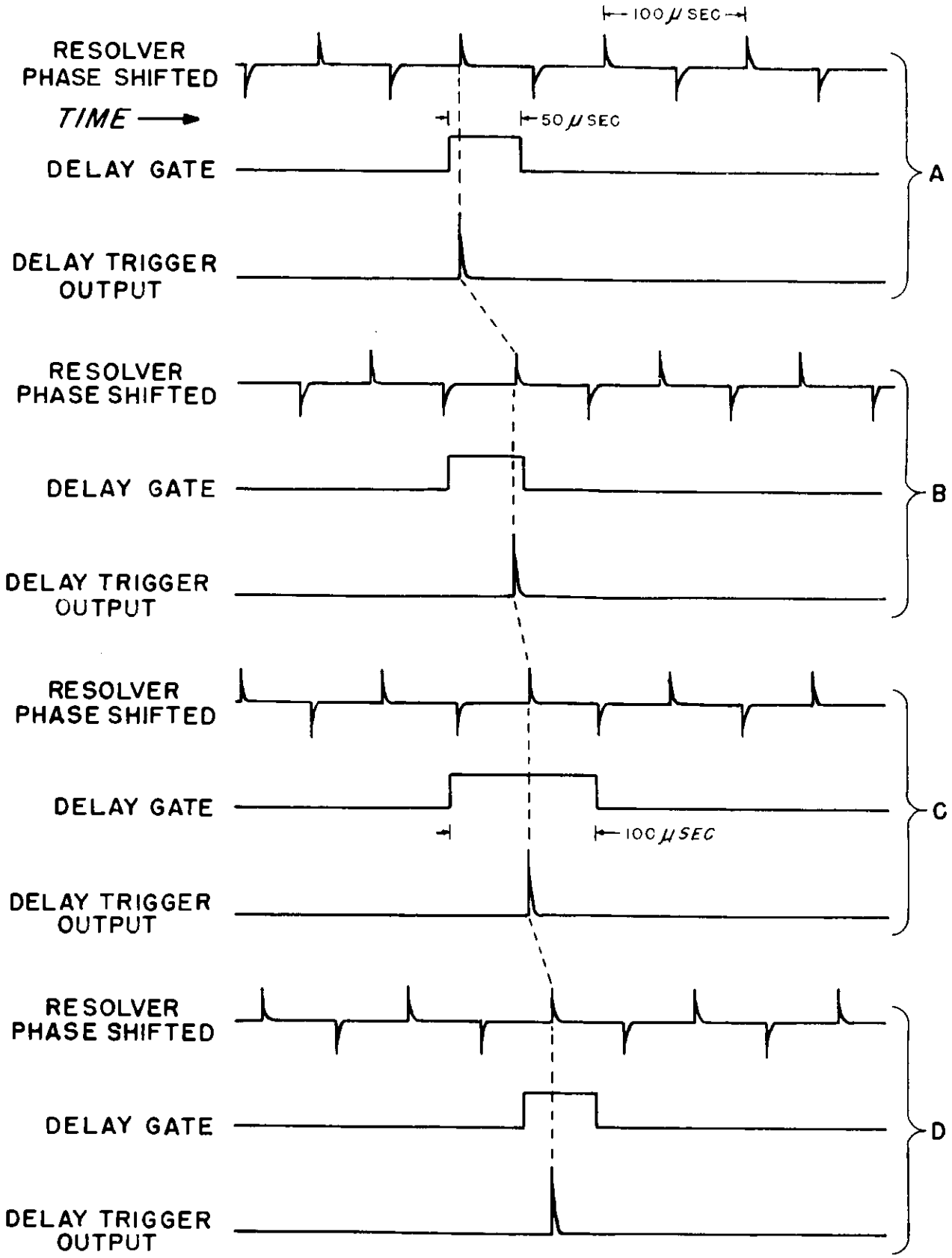


Figure 24

BASIC DELAY SYSTEM OPERATION

An output from the third counter is fed through the third counter limiter, V118, where it is amplified and then converted to a sine wave by the tuned tank, L104. L104 is tuned to 10 kc which passes only the fundamental of the 10 kc square wave (100 microseconds). The sine wave is amplified in V118B and fed through a cathode follower, V119A, where it is applied to the phase shifting resolver, B101.

The resolver has a single phase rotor (the red and black input leads on the master schematic) and two equal stator windings which are wound 90° apart mechanically. If either secondary (stator) winding is fully in phase with the input winding and produces maximum output, the other winding will be 90° apart from it (and hence the input winding) and therefore, its output will be zero. If the resolver rotor is rotated 90°, the condition just mentioned will be reversed, that is, the winding that formerly had maximum output now has 0 output and the winding formerly 0 now has maximum output.

The outputs of the two windings are added together through C147 and R201 and R202. If R201 is adjusted so that R201 and R202 equals the impedance of C147 at 10 kc, then the resultant output will be constantly phase shifted, constant amplitude 10 kc sine wave. Notice that for the phase shift to work properly, the impedance of C147 and R201 must be equal at 10 kc. That is the reason for converting the 10 kc square wave to a 10 kc sine wave so that only the fundamental would appear at the resolver windings.

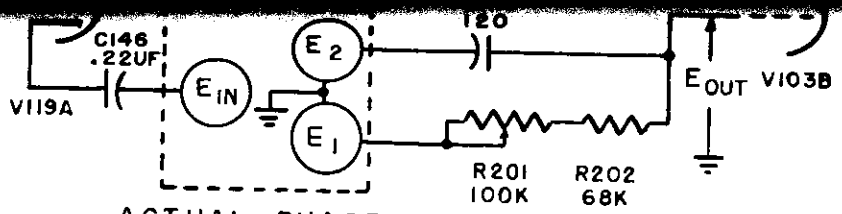
Figure 25 is a simplified version of the resolver phase shift circuit, and 5 positions of rotation are shown to illustrate the phase movement of the output with respect to the input.

Since R201 is adjusted to match C147, never indiscriminately turn this control. A locknut is provided on the potentiometer for this reason. Proper adjustment of the control is made, when by turning the DELAY crank rapidly (and hence, the resolver), minimum amplitude variation of sine wave occurs on an oscilloscope at TP105 (indicating equal resistance and capacitive reactance).

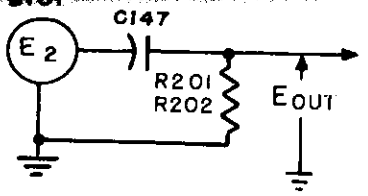
The constant amplitude, constantly phase shifted since wave, is amplified in V103B and V120. The output of V120, pin 6 is a 10 kc (100 microsecond) square wave which is differentiated by C152 and R351 into a series of positive and negative pulses which are fed to the grid of the delay pulse generator, V142.

Since the positive phase shifted pulses are 100 microseconds apart, each time the TIME DIFFERENCE dial changes in reading by 100, the resolver has made one complete revolution. As previously explained, the first set of DELAY switches S105A and S105B completes one revolution in 400 microseconds. Therefore, there is a gear reduction of 4:1 between the resolver (and TIME DIFFERENCE dial) and the first set of DELAY switches. This is shown in Figure 23.

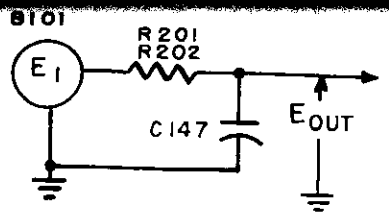
Notice from the master schematic that in addition to the phase shifted 100 microsecond pulses, the 50 or 100 microsecond positive delay gate is also applied to the grid of the delay pulse generator, V142. Thus, the two signals are mixed at the grid of V142.



ACTUAL PHASE SHIFTER , B101, CIRCUIT



EQUIVALENT CKT OF B101 IN POSITION OF 90° ROTATION



EQUIVALENT CKT OF B101 IN POSITION OF 0° ROTATION

ROTATION	PHYSICAL POSITION OF STATOR WITH RESPECT TO ROTOR	E_{IN}	E_1	E_2	E_C	E_R	E_{OUT} (EQUALS $E_R + E_C$)
0°				0		0	
45°							
90°			0		0		
135°							
180°				0		0	

Figure 25 VECTOR ANALYSIS OF RESOLVER PHASE SHIFT

This tube is a thyratron similar in operation to the PRR reset generator. The grid is held cut off by a fixed bias developed by R354 and R353. Only when a combination of positive pulse atop the positive delay gate occurs will the thyratron fire. This produces a sharp positive delay pulse at the cathode of V142 which is fed to the grid of the pedestal generator, V143, to develop the delay pedestal.

Figure 26 shows various TIME DIFFERENCE readings from 2015 to 2115. This represents a change of 100 microseconds which equals one full revolution of the resolver; 90° revolution of S105A and S105B, 22.5° of S105C and S105D, etc.

Notice that in A, the resolver phase shifted pulse is approximately $\frac{1}{4}$ across the delay gate. Waveform B is an intermediate position of the pulse atop the gate. In C, the TIME DIFFERENCE dial has change 25 microseconds and, therefore, the delay gate has changed to 100 microseconds. (Refer back to Figure 18 which shows that the 50 or 100 microsecond delay gate output alternately changes every 25 microsecond change of the dial.)

The delay gate, in becoming 100 microseconds wide, allows the phase shifted pulse to move from C to D. Notice that the pulse has now passed over the original 50 microsecond part of the gate. At E (a change of 25 from C) the delay gate narrows to 50 microseconds but the pulse is still atop the gate so that a delay trigger will always be generated. If, because of some misalignment, anywhere within the range of delay readings 0000 to greater than 10,000, the delay pedestal disappears, it can only be caused by not having the right combination of delay pulse atop delay gate.

Notice that whenever the delay gate changes (from a 50 to 100 or vice versa), the delay pulse is always well removed from either front or rear edge of the gate. This is done to provide a wide tolerance in angular positioning of the switches without adversely affecting the operation or accuracy of the equipment. (Notice that the accuracy of the system is determined solely by the revolver pulse; the gate merely selects the proper pulse to be used.

In explaining the development of the delay gate, it was shown that a delay of 1600 microseconds from reset is provided for convenience in viewing the master pedestal. Therefore, 1600 microseconds had to be subtracted from the delay pedestal readings. For a TIME DIFFERENCE of 0000, the delay pedestal must be 1600 microseconds removed from its reset. In addition to this 1600 microseconds, there is an additional 13 microsecond delay provided because proper positioning of the phase shifted pulse places it 13 microseconds from the edge of the delay gate.

Therefore, when the DELAY crank is rotated to its counterclockwise stop, the TIME DIFFERENCE dial reads 98387. This number is 1613 microseconds less than a reading of 0000. This number, 98387, is the reading when delay gate occurs at delay reset. By moving the dial 1613 microseconds, the dial will read 0000 and the delay pedestal will be removed from its reset the same amount the master pedestal is delayed from its reset.

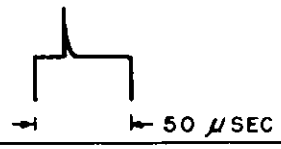
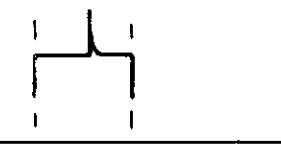
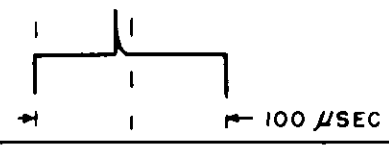
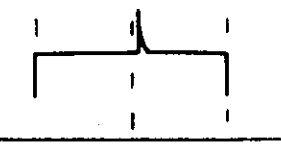
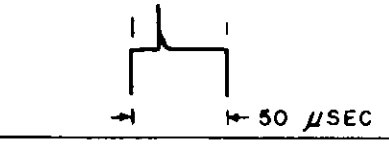
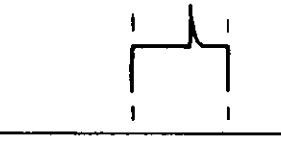
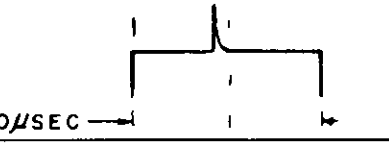
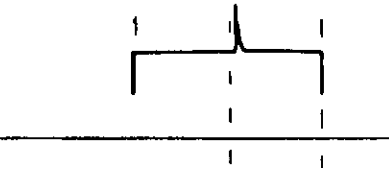
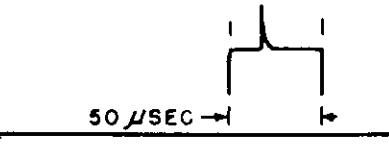
	DELAY PULSE GENERATOR INPUT	TIME DIFFERENCE (Typical reading)	RESOLVER RELATIVE ROTATION (100 μsec phase shift)
A		2015	0°
B		2030	54°
C		2040	90°
D		2055	144°
E		2065	180°
F		2080	234°
G		2090	270°
H		2105	306°
J		2115	360° or 0°

Figure 26
RELATIONSHIP OF DELAY SYSTEM AND TIME DIFFERENCE DIAL

The explanation of the delay system is complete, but a few small points which are not concerned with the explanation of the delay system will be explained.

(1) Notice that an output from the twelfth counter cathode follower, V125A is fed to the third delay coincidence amplifier, V119B. This square wave prevents a delay pedestal from occurring during the master trace and allows the delay gate to be developed only during the slave trace.

(2) Notice that the common plates of the delay gate tubes, V136, V138, V139 and V141 each has a capacitor to ground connected to it. The purpose of each of these condensers is best explained by Figure 27. Notice in A and B the sharp edges of the delay gate when no condenser is used. However, notice in B that there is a hole developed when a 100 microsecond gate is obtained. If the hole were allowed to remain, there would be the possibility that the phase shifted pulse might fall in this hole as the DELAY crank is rotated. Thus, the positive pulse atop the delay gate would in effect be falling in a notch, and the bias of the delay pulse generator tube, V142, might not be overcome. The delay pedestal would then disappear. To prevent this from happening, capacitors are placed on the plates of the delay gate tubes resulting in waveform C, which rounds the edges of the gates as well as reducing the hole markedly. The phase shifted pulse will now ride smoothly atop the gate.

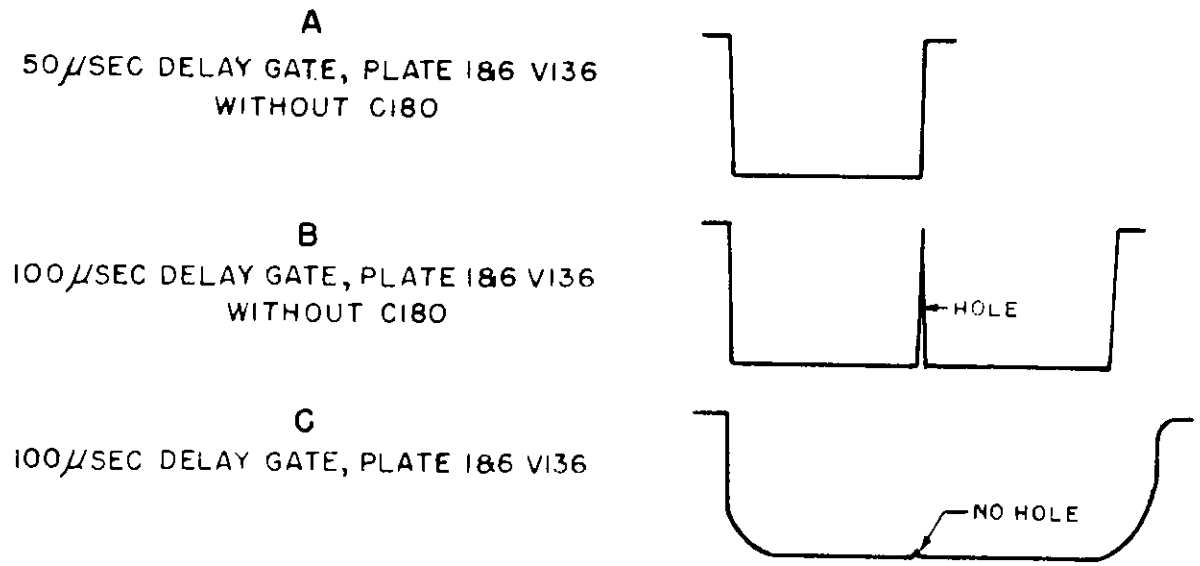


Figure 27
DELAY GATE WAVE SHAPING

CHAPTER V
ALIGNMENT PROCEDURES

18. ALIGNMENT PROCEDURES

Chapter II, Sections 11 thru 11.6 described initial adjustments and checks which should be performed on newly-installed equipment. These same checks should be made periodically to determine if the LR-8803 is functioning properly, and they should be performed after every major repair or service work.

The alignment procedures described in the following sections should normally be performed only if critical parts have been replaced, or if a complete overhaul of the LR-8803 is required.

18.1 RECEIVER ALIGNMENT

Necessary Test Equipment

1. Signal Generator (accurately calibrated from 1100 kcs to 2000 kcs) or Loran Pulser, Model TS-251/UP.

2. Voltohmmeter. Simpson Model 260 or equivalent meter having at least 20,000 ohms/volt resistance on DC scales.

3. Damping load consisting of ½w, 470 ohm resistor and ceramic disc .01 mfd capacitor in series.

A. I.F. Alignment

Set the receiver controls to the positions indicated below:

GAIN ..... ½ scale (approx. -7.5 volts bias)
CHANNEL ..... CHANNEL 1
BALANCE ..... center of range
LOCAL-DISTANT .. DISTANT

Attach voltmeter to the detector output jack, TP501, and set meter on 10 volt DC range. Connect signal generator to antenna input jack at rear of receiver (J501).

Turn power ON and allow a 10 minute warm-up for all equipment.

Feed an input signal of 1950 kc, unmodulated carrier into LR-8803.

Note 1: The signal generator used for this alignment must be accurately calibrated in frequency. A signal generator which is inaccurate in frequency calibration will result in misalignment of the Loran receiver.

Note 2: The Loran Pulser, TS-251/UP is an excellent source of crystal controlled RF power for this alignment, and should be used where possible. When the OUTPUT SELECTOR switch is thrown to the clockwise position, outputs of 15 microvolts, 1 millivolt and 1 volt can be obtained.

Now damp the primary winding of the final IF transformer, T505, by shunting it with the resistor-capacitor combination.

Tune the secondary of this transformer (all secondary tuning slugs are accessible from the bottom of the chassis) for maximum deflection of the detector meter. Starting with the slug all the way out, the first peak obtained is the proper one. By means of the amplitude control on the signal generator (or TS-251/UP), keep the detector output near 10 volts throughout the tuning procedure. Remove damping from primary of final IF tank. Damp secondary by connecting the resistor-capacitor combination across secondary. Tune primary for peak. (All primary slugs are on top of receiver transformers.) Starting with slug all the way out, the first peak is the one to be used. Remove damping from secondary.

In like manner tune the remaining IF transformers, T504 and T503.

After all IF transformers have been peaked, remove the damping load and check the over-all IF band pass if an accurately calibrated signal generator is available. This can be done by feeding a 1100 kc signal into pin 7 of V502 and measuring the bandwidth to the 3 db points. Bandwidth should be approximately 40 kcs. IF transformers may be trimmed very slightly to obtain the desired symmetry.

B. R.F. Alignment (CHANNEL 1)

With RF source set at 1950 kcs and using the same set-up as previously described for IF alignment, connect damping load to secondary of T502 and tune primary inductance to give maximum response on the voltmeter at TP501. Output level should be approximately 10 volts.

Remove damping load and connect to primary of T502 and tune the secondary inductance for peak.

In like manner tune secondary inductance of T501.

To tune primary inductance of T501, remove damping load and tune primary for maximum output at detector load.

C. R.F. Alignment (CHANNEL 2)

With band switch on CHANNEL 2 and using same set-up as described above, set signal generator or test set to give an RF output of 1850 kcs. The receiver GAIN control is set at -7.5 volts and the RF source is adjusted for approximately 10 volts at the detector jack. Connect the damping load to the secondary of T502 and tune trimmer capacitor, C507, for peak output on the voltmeter. Then connect damping load to primary of T502 and tune capacitor C516 for peak output.

Finally, connect damping load to primary of T501 and tune capacitor C503 for peak output. Note: Do not re-tune any inductances since they have all been tuned for CHANNEL 1.

D. R.F. Alignment (CHANNELS 3 and 4)

In a manner similar to that described in Paragraph C, tune the RF stages for CHANNEL 3, 1900 kcs and CHANNEL 4, 1750 kcs.

For CHANNEL 3 the trimmer capacitor across the primary of T502 is C506, and the trimmer across the secondary is C515. For T501, the trimmer used is C502.

When aligning CHANNEL 4, the primary trimmer for T502 is C505 and the secondary trimmer is C513. The trimmer for T501 is C501.

E. I.F. Trap Alignment

With a 1100 kc signal fed into antenna jack and receiver gain at maximum, tune L501 for minimum output at detector jack, TP501.

18.2 ALIGNMENT OF 80 KC CRYSTAL OSCILLATOR AND REACTANCE TUBES (L101 AND L102)

Before making adjustments to L101 and L102, allow a minimum of 10 minutes warm-up time for the equipment. This will allow complete stabilization of V101 and V102 so that when adjustments to L101 and L102 are made, they will be correct.

With an oscilloscope probe connected to TP101, set the DRIFT knob in the OUT position and in its center of rotation. Adjust oscillator plate coil, L102, and notice that the sine wave appearing on the oscilloscope increases in amplitude until the point is reached where the sine wave suddenly collapses to zero. From this position, back out the coil slug approximately 2 turns. The sine wave should reappear and should be approximately 75% maximum amplitude.

Disconnect the oscilloscope probe. If signals are present, connect the antenna to the receiver. If no signals are present, connect Loran Test Set TS-251/UP to the receiver. Set the RATE switch to the correct rate which should stop signals on FUNCTION 1. The signals should appear almost stationary on the two traces. Using the LEFT-RIGHT switch, place a signal on the master pedestal (a signal on the DELAY pedestal is not required).

Turn FUNCTION switch to FUNCTION 2. Rotate DRIFT knob from extreme clockwise to extreme counterclockwise position and notice the speed with which the signals move across the screen. For extreme limits of the knob, the signals should drift across the screen at equal speeds to the left and right. (Note: FUNCTION 2 sweep is recommended in making this adjustment because the speed with which the signals drift across the screen most readily indicates any unbalance between the limits. However, in making the check the signal may drift off the trace and disappear. In such a case, use the LEFT-RIGHT switch to bring it back on the trace.)

If equal drift to the left and right is not obtained as the knob is rotated through its limits, adjust the reactance tube plate coil, L101, until equal limits of drift is obtained.

Note: A certain amount of caution should be exercised when making the aforementioned adjustments. As the schematic diagram indicates, it is possible for L101 and L102 to form a tuned-plate, tuned-grid oscillator. If both coils are improperly tuned, the circuit will no longer oscillate as a crystal oscillator at 80 kc but as a tuned-plate, tuned-grid oscillator at a frequency far enough removed from 80 kc to prevent stopping signals. It is also possible that improper adjustment of L101 will cause the circuit to operate properly over part of the DRIFT knob rotation, but improperly over the rest of the knob rotation.

Be certain that final adjustment of L101 is made using signals whereby the signals drift equally to left and right for the extremes of the DRIFT knob.

18.3 ADJUSTMENT OF RESOLVER BALANCE POTENTIOMETER (R201)

Place the probe of an oscilloscope on TP105 (V120 pin 2). A 10 kc sine wave should appear. Adjust the oscilloscope to observe at least 25 cycles of the sine wave.

Adjust L104 (V118 pin 7) for maximum sine wave on the oscilloscope. (The coil Q is low and the amplitude change with tuning is very broad.)

With DELAY crank in high speed, rotate the crank rapidly. If the RESOLVER potentiometer, R201, is incorrectly adjusted, an amplitude variation will be observed on the oscilloscope. Loosen the lock nut and adjust the RESOLVER potentiometer until minimum amplitude variation is observed as the DELAY crank is rotated. LOCK THE POTENTIOMETER.

18.4 ADJUSTMENT OF RESOLVER PHASE SHIFT

Using the TS-251/UP test pulser, feed in test signal to the LR-8803. Set the RATE switch on the Indicator to receive one of the test signals (say H3). Place the TIME DIFFERENCE dial to the reading which should normally match the first two signals (that is, 1650 microseconds if the H3 signals are being used). With the FUNCTION switch on POSITION 3, and the AFC-DRIFT switch on AFC, the two signals should be matched.

If the two signals do not coincide to within ±1 microsecond, proceed with the following:

Procedure A.

1. Set FUNCTION switch to FUNCTION 3.
2. Set TIME DIFFERENCE dial to 1650 microseconds (with LR-8803 adjusted to use H3 signals).
3. Loosen the two screws that clamp the resolver body.

4. Now turn the resolver body until the first two signals from the TS-251/UP pulser coincide. It may be necessary to hold the TIME DIFFERENCE drum at 1650 microseconds by hand to prevent it from turning.

5. Tighten the two screws to secure the resolver body.

6. Turn to FUNCTION 1 position and see if the first two signals from the pulser are atop the master and slave pedestal respectively for a TIME DIFFERENCE setting of 1650 microseconds.

7. Turn to FUNCTION 3 and match the two signals. If the TIME DIFFERENCE is still greater than plus or minus 1 microsecond in error, repeat the above procedure.

Note: It is possible, but not very likely, that the two signals may be off by more than 100 microseconds on the TIME DIFFERENCE dial when a match is made. This means that the resolver pulse is atop the wrong delay gate which is due to misalignment between the gear box and the delay switch mechanism. This misalignment can be caused by the coupling between the gear box and delay switches being loose. If errors greater than 100 microseconds are encountered, use the following alignment procedure.

Procedure B

1. Turn the resolver shaft according to the directions given in Procedure A so that the first two signals from the TS-251/UP test set coincide. Note that the TIME DIFFERENCE will now read 100, 200, 300 microseconds, etc. from the correct value (should read 1650 microseconds for H3 signals).

2. Tighten the screws that secure the resolver.

3. Now loosen the coupling between the gear box and the delay switch mechanism.

4. Turn the DELAY knob until the TIME DIFFERENCE reading is at the correct value.

5. Tighten coupling between gear box and delay switches.

Example: With the LR-8803 set to receive H3 signals from the TS-251/UP, the TIME DIFFERENCE reading is 1455 microseconds when the first two signals are matched. Since the TIME DIFFERENCE should be 1650 microseconds, this means that the error is 195 microseconds. Now we can get the two signals to match (see Step 1 of Procedure B) by turning the resolver body. Match will then occur at 1450 microseconds of the TIME DIFFERENCE dial (200 microsecond error). Now tighten resolver body. Loosen coupling between gear box and delay switch mechanism and move the DELAY crank until the TIME DIFFERENCE reads 1650 microseconds. Tighten coupling.

It should be noted here that the resolver phase shift alignment can be checked by use of the SELF-CHECK circuit (see Section 11.4, Steps 16, 17, 18 and 19). When the phase shift circuits are in alignment, the SELF-CHECK wave will coincide as the TIME DIFFERENCE dial passes through numbers ending in 00. If the SELF-CHECK waves do not coincide for 00 readings, align by the following method.

1. Set the TIME DIFFERENCE dial to any number ending in 00.

2. Loosen the two screws that hold the resolver body.

3. Turn the body of the resolver until the SELF-CHECK waves coincide. It may be necessary to hold the TIME DIFFERENCE drum by hand at the 00 reading to prevent it from turning.

4. Tighten the two screws.

Note that using the SELF-CHECK to align the resolver phase shift circui does not give us any information as to whether the resolver pulses are atop correct delay gate. In other words, even if the resolver is aligned properl by means of the SELF-CHECK circuits, there could be time difference errors o 100, 200, 300 microseconds, etc. The only way to be sure that the resolver pulses are atop the correct delay gate is to use the TS-251/UP test set acco ing to the directions given in Procedure A of Section 18.4.

18.5 POSITIONING THE PHASE SHIFTED PULSE PROPERLY ATOP THE DELAY GATE

In Section 18.4, directions were given for aligning the resolver pulse top of the correct delay pulse. Such alignment does not indicator, however, that the resolver pulse is positioned at the proper point on the correct del pulse. This positioning will now be discussed.

Set the FUNCTION switch in FUNCTION 2 position and the AFC-DRIFT contr in the DRIFT position. Drift a signal on to the bottom trace of the 'scope rotate the DELAY crank in low speed for approximately 500 microseconds. Ob the movement of the signal across the trace. Movement should be smooth and steady with no erratic motion. If jumpy or erratic motion occurs, correct the following procedure.

1. Place the probe of an oscilloscope at TP111 (grid 1 of V142, delay pulse generator). Use external sync, if possible, for the oscilloscope and place the external sync lead at TP103 (plate 6, V116, PRR reset generator).

2. Expand the picture shown in Figure 28, Line A by adjusting the horizontal frequency control of the test oscillscope. The picture desired is one which will show the delay gate as in Figure 28, Line B. Depending on the oscilloscope used, this may be a bit difficult since we are trying to view a

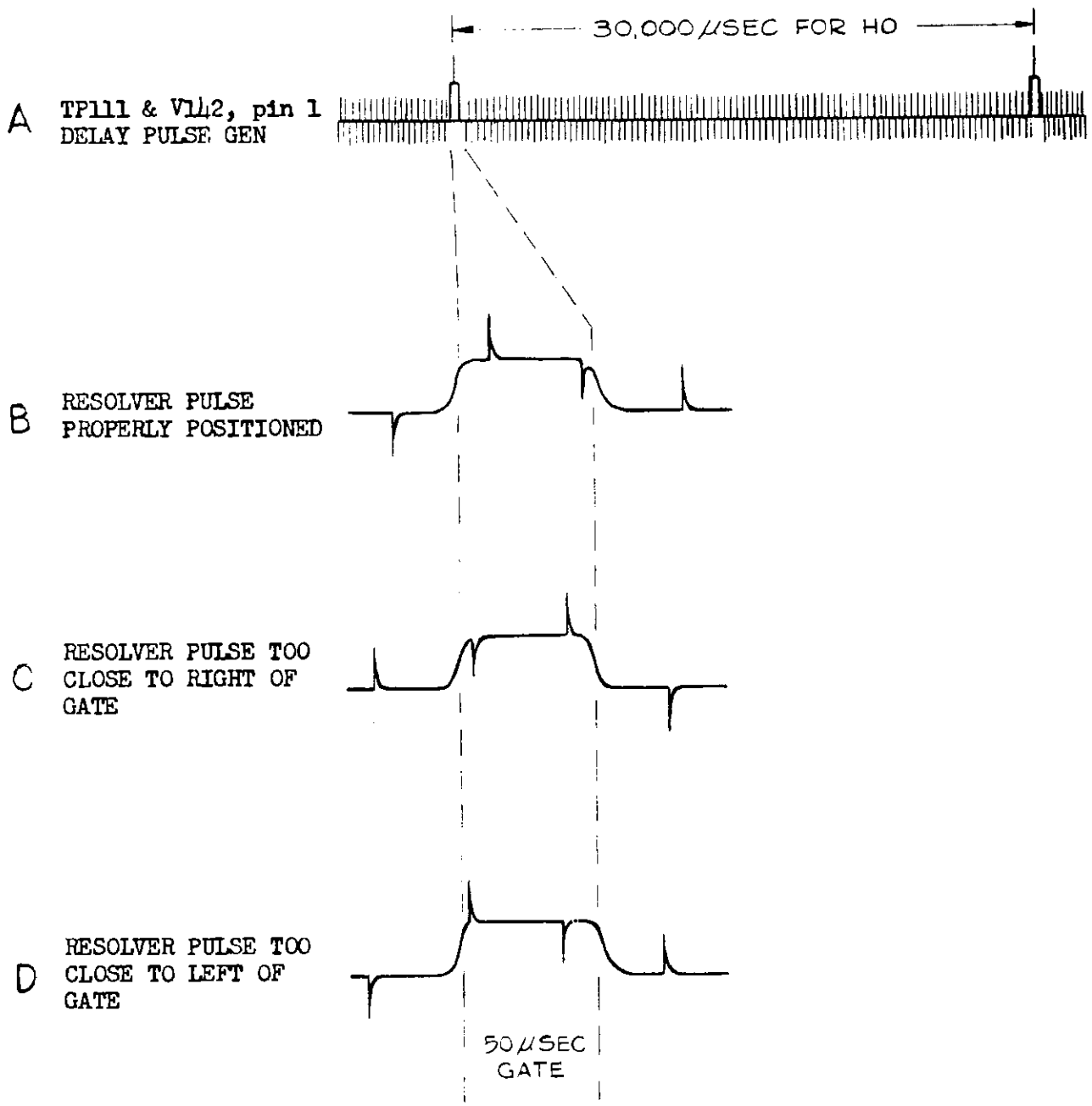


Figure 28

PROPER POSITIONING OF RESOLVER PHASE SHIFT PULSE ON DELAY GATE

100 microsecond gate (Figure 28, Line B) as a part of a full 15,000 microsecond loran cycle (Figure 28, Line A). In adjusting the oscilloscope to give the picture shown in Figure 28, Line B, do not be concerned if a clean baseline is not obtained. What is important is to enlarge the delay gate as much as possible and to have the delay gate stationary on the oscilloscope. In this manner it is easier to position the phase shift pulse atop the delay gate.

3. Rotate the DELAY crank to any reading above 00000 whereby the wide (100 microsecond) gate has just been switched to a narrow (50 microsecond) gate (as seen on the oscilloscope). Loosen the front screws on the coupling between the gear box output and the delay switch input. This disengages the DELAY switch from the gear box.

4. Rotate the DELAY crank (slow speed) a small amount, not more than 15-20 microseconds maximum time difference change and observe the position of the pulse atop the gate. The correct position of the pulse atop the gate is that shown in Figure 28, Line B (for the condition when the DELAY switch is adjusted to produce a 50 microsecond gate as mentioned above).

5. When the pulse is properly positioned, tighten the screws on the coupling between the gear box output shaft and delay switch input shaft.

To assure that the pulse is properly positioned for any TIME DIFFERENCE reading, turn to SELF-CHECK, FUNCTION 3. Rotate the DELAY crank slowly for a few hundred microseconds and observe that a smooth movement of one set of square waves across the screen results. If anywhere in this range, the square waves either jump or disappear momentarily, then the pulse is not positioned properly and must be repositioned. Be sure to rotate the DELAY crank in both directions for if the pulse is near either edge of the gate, it is possible for all to be normal in one direction, but jumpy in the other direction of rotation. When smooth movement results, the delay system is completely aligned. Return SELF CHECK to NORMAL.

CHAPTER VI
MAINTENANCE

19. EMERGENCY MAINTENANCE

Defective fuses and tubes account for a great many of the failures in electronic equipment and, therefore, the operator or service technician should check these items first when the loran equipment is not functioning properly.

19.1 FUSE LOCATION AND FAILURE CHART

Never replace a fuse with one of higher rating. If a fuse burns out immediately after replacement, do not replace it a second time until the cause has been corrected.

CHART I. FUSE LOCATION AND FAILURE SYMPTOMS

Fuse Location	Type	Failure Symptom
F601 - RM-218	AGC - 1 amp	Blank CRT picture for all functions. Panel lighting OK.
F602 - RM-218	AGC - 5 amp	Panel light OK. No +160, +260, -105 or H.V.
F701 - RM-219	AGC - 2 amp	Panel light OK. No indicator heaters lighted.
F702 - RM-219	AGC - 2 amp	Panel light OK. No indicator heaters lighted.
F101 - Indicator	AGC - 1 amp	No panel lighting. CRT picture normal.

19.2 TUBE REPLACEMENT

Do not change tubes indiscriminately, but when possible, localize trouble to a specific circuit by means of the procedures given in Section 21.1 of this chapter. It is important to change only one tube at a time and to make certain that the correct type is placed in the correct socket Each socket is marked with the tube type, and Figure 29 shows the tube type and location for all tubes in the Indicator-Receiver unit. There are 9 tubes in the RM-218 Power Supply, all of which can be located easily by means of the chassis markings. The RM-219 Junction Box and the RM-220 Coupling Unit contain no tubes.

19.3 BLOWER

The blower motor, in the blower housing at the rear of the cabinet, is permanently lubricated. However, from time to time the blower motor and fan should be wiped free of accumulated dust and the filter washed in a detergent before being replaced. The filter is easily removed by taking out two screws at the top and two at the bottom of the blower housing.

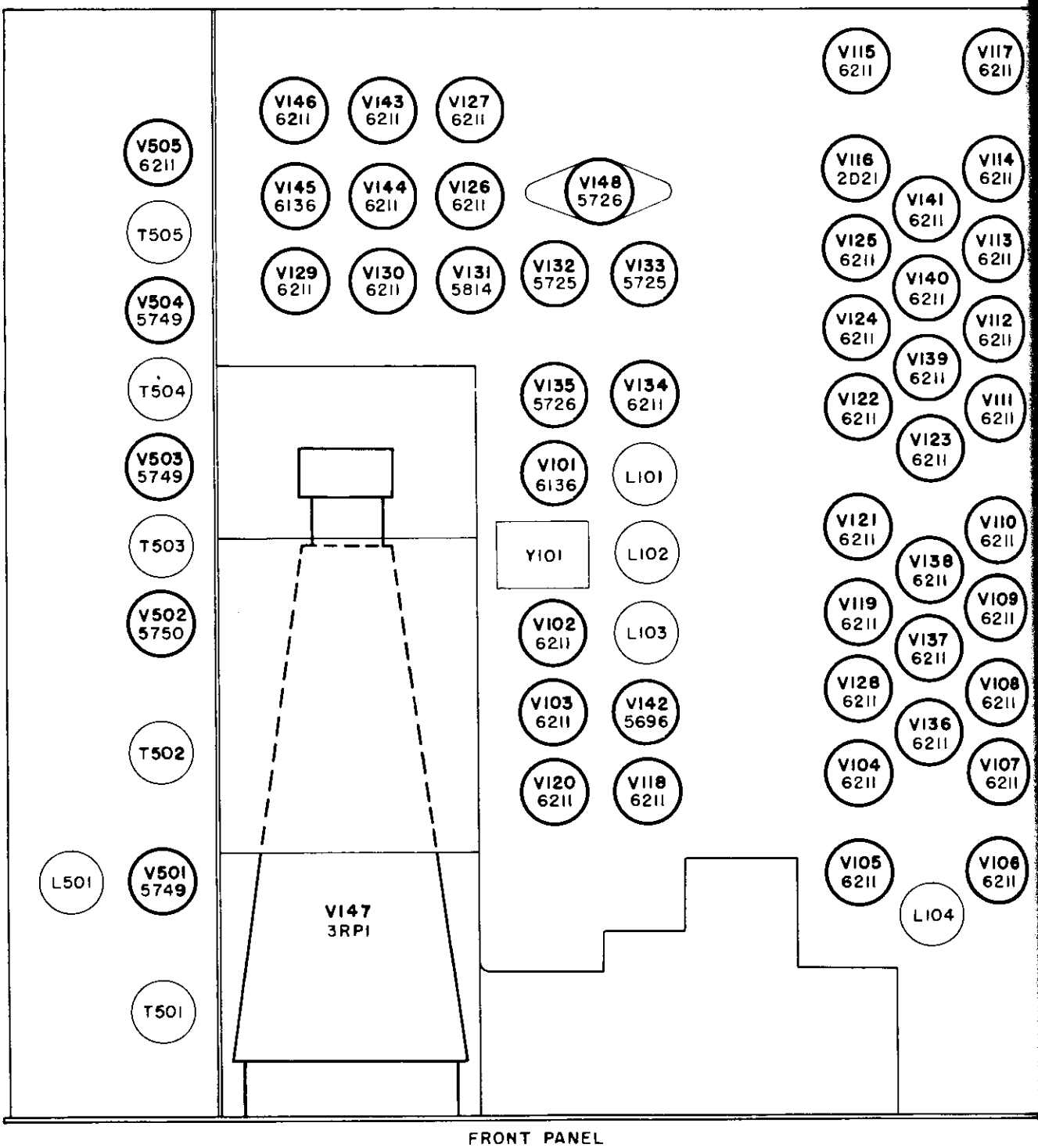
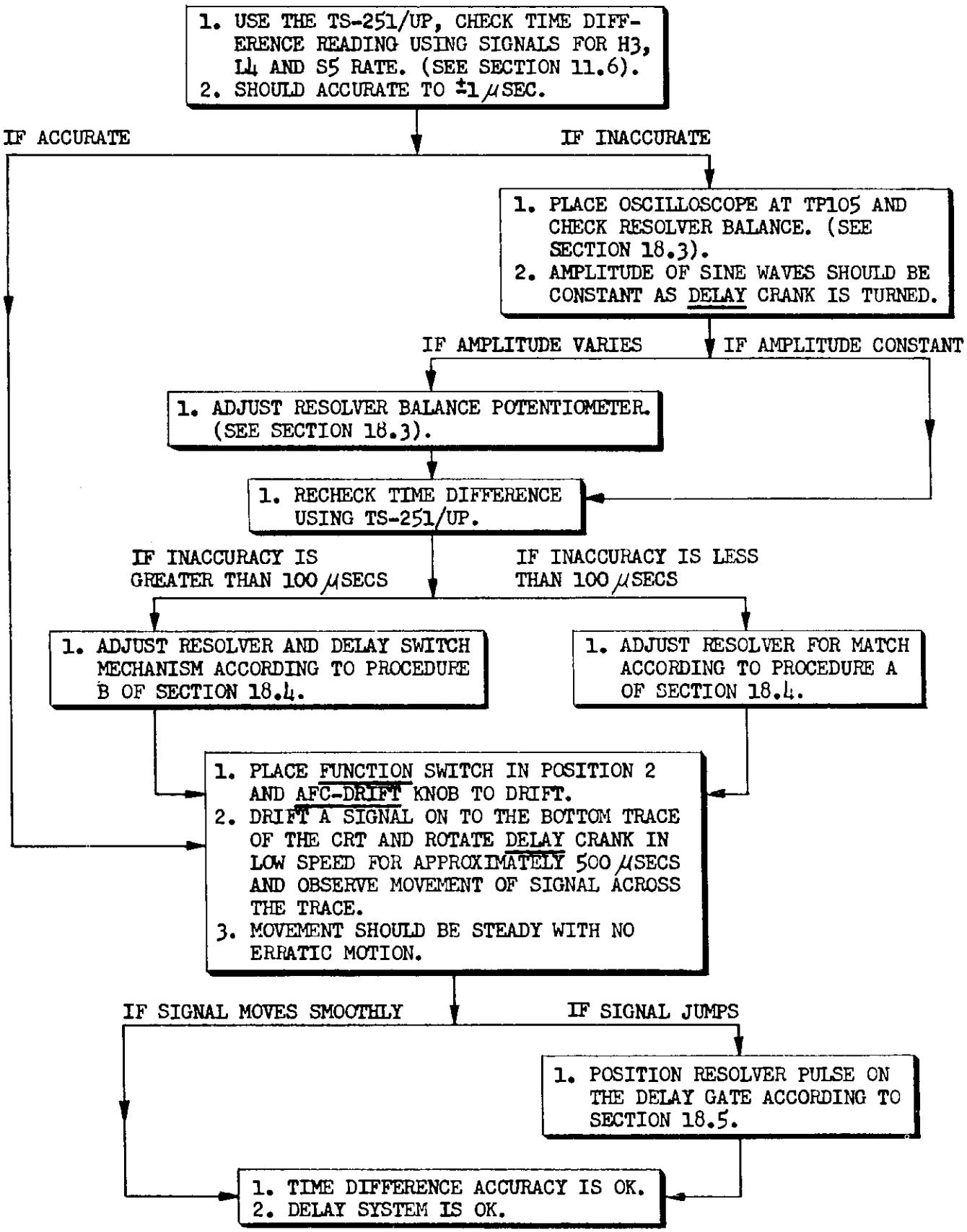


Figure 29

TUBE LOCATION DIAGRAM OF INDICATOR-RECEIVER

CHART II

Alignment Procedure and Trouble - Shooting Chart for Delay System.



C A U T I O N

1. Always turn the POWER switch OFF before changing tubes.

2. Be careful not to touch the high voltage circuits. Although these circuits contain bleeders, after power is removed always discharge and ground such circuits prior to touching them.

20. ROUTINE MAINTENANCE

The serviceman should make periodic checks of the following characteristics according to the directions given in the referenced sections.

	WHAT TO CHECK	HOW TO CHECK
(1)	Power Supply Voltages	See Section 11.3
(2)	Counter Bias	See Section 11.4, Step 15
(3)	Time Difference Accuracy	See Section 11.6
(4)	Switch S-105	Frayed or poorly dressed jumper

Item (3) is a most important check since any inaccuracy of the delay system can be determined by this means. The TS-251/UP Test Set must be used for this check. See Chart II for maintenance procedures to be followed if there is any error discovered in the time difference reading.

21. TROUBLE SHOOTING

Troubles in the LR-8803 Loran set can often be located by means of the Trouble Shooting Charts in the following sections.

21.1 TUBE TROUBLE CHART

When using the following tube trouble chart, turn the operating controls to the positions shown below unless other settings are called for in the column of the chart marked "Symptoms of Failure".

Control	Position
LOCAL-DISTANT	DISTANT
INTERFERENCE REDUCER	OFF
BALANCE	0
CHANNEL	1
GAIN	5
RATE	H3
TIME DIFFERENCE	1650.
IN AFC-OUT DRIFT	DRIFT (MANUAL)
FUNCTION	1

CHART III. TUBE FAILURE SYMPTOMS

Picture Symptoms of Failure	Other Symptoms	Faulty Tube (any one or more)
Signals drift slowly and cannot be stopped in Function 1, 2 and 3.	No manual drift or automatic frequency control.	V101
A spot or vertical line is seen at center of CRT in Function 1 and is seen at the left side of CRT in Function 2 and 3.		V102 thru V115, V601, V605, V608
A single trace with no pedestals in Function 1 and a vertical line on left side of CRT in Function 2 and 3.	Signals will stop and can be drifted left or right.	V117
No slave pedestal in Function 1, and a single trace in Function 2 and 3.		V118
An intermittent slave pedestal on master and slave trace when time difference dial is rotated past 2900 microseconds.	In Function 2 and 3 the slave trace becomes intermittent.	V119
An intermittent slave pedestal when time difference dial is rotated.	In Function 2 and 3 the slave trace becomes intermittent.	V120
Signals do not lock in on proper rate.	Rate switch on rate of known signals.	V121 thru V124
No gain or balance control.	Picture normal except for some increase in noise level.	V126
Single trace and no pedestal in Function 1. Vertical line on left side of CRT in Function 2 and 3.		V125

CHART III. TUBE FAILURE SYMPTOMS (cont'd)

Picture Symptoms of Failure	Other Symptoms	Faulty Tube (any one or more)
No trace separation and no pedestals on Function 1. No trace separation in Function 2.		V127
No master pedestal in Function 1 and a single trace in Function 2 and 3.		V128
AFC will not "lock-in" signals. Manual (drift) operation normal.		V129, V130, V134, V135
No signals and no grass.	**No self check.**	V131
Signals will "lock-in" on AFC only over one end of drift knob rotation. Manual operation normal.		V132, V133
No delay (or slave) pedestal in Function 1 and no delay (or slave) trace in Function 2 and 3.		V136, V138, V139, V141, V142
Delay pedestal skips along when time difference dial is rotated in Function 1. Intermittent delay trace in Function 2.		V137
Delay pedestal skips back as time difference dial is rotated in Function 1.		V140
No pedestals in Function 1 and a vertical line on left side of CRT in Function 2 and 3.		V143
Horizontal amplitude decreased in Function 1. Picture not focused in Function 2 and 3.		V144

CHART III. TUBE FAILURE SYMPTOMS (cont'd)

Picture Symptoms of Failure	Other Symptoms	Faulty Tube (any one or more)
Two vertical lines at center of CRT in Function 1. Two vertical lines at left side of CRT in Function 2. A vertical line at left side of CRT in Function 3.		V145
No master pedestal in Function 1 and no master trace in Function 2 and 3.		V146
Nothing (blank CRT).		V609, V147
Excessive brightness and picture not in focus.		V148
No signals but some noise present when gain is maximum.	Picture otherwise normal.	V501
No signals or noise present.	Picture otherwise normal.	V502 thru V505
Spot in center of CRT when in Function 1, 2 and 3.		V602, V603
60 cycle ripple on sweeps and the time difference when rotated, causes an intermittent slave pedestal.		V604
The picture is not in focus and there are many pedestals present that skip around.		V606
Single trace, horizontal trace very low in Function 1, 2 and 3.	Some noise present.	V607

21.2 TEST POINT AND WAVEFORM CHART

There are 13 test jacks on the Indicator-Receiver unit which should be used as an aid in aligning and servicing the equipment. The location of these test points are shown in Figure 1.

With the exception of TP102, each of these test points has a waveform output which can be viewed on an oscilloscope with a vertical amplifier at least 5 megacycles wide. A Tektronix model 524A, or equal, is recommended.

Note: A proper oscilloscope must be used for this work. A poor oscilloscope will not only give improper pictures, but will cause mis-adjustment if used for alignment.

These test point waveforms are shown on Chart IV at the end of this chapter. To observe them, set the controls of the Indicator-Receiver as listed in the directions which precede this chart. For some of the waveforms, the position of certain controls must be changed according to the data given under a specific waveform. In those cases where signals are required, use Loran Test Set TS-251/UP.

The test point and waveform chart also shows many other voltage waveforms which are obtained at various points in the Indicator-Receiver. These should be used in trouble shooting to trace a source of trouble to a specific stage.

As an aid in finding trouble, the voltage waveforms of test points TP107, TP108, TP109 and TP110 are especially valuable for the following reason:- if trouble develops which results in only a spot or vertical line on the cathode ray tube screen, a common source of trouble is the binary counter chain. To check the operation of the binary counters, observe the output of TP107 on an oscilloscope. This test point will check the 3rd, 4th and 5th counter. Figure 30, Line A shows the correct pattern if the 3rd, 4th and 5th counters are operating properly. Do not be concerned with the exact shape of the waveform, but be sure there are four and only four levels on the oscilloscope as shown in Figure 30. If only 3 levels are present (as shown in Line B of Figure 30) then the 5th counter is inoperative. If only 2 levels (a square wave) appear (Line C, Figure 30), then the 4th counter is inoperative. If no output appears then the 3rd counter is inoperative (or the 2nd or 1st counter or preceding circuits up to the crystal oscillator).

If the output of TP107 has the correct output of 4 levels, then move to TP108 and check in a similar manner for the correct output of 4 levels. If they are present, move to TP109 and check it for 4 levels. The trouble is localized to a particular group of 3 counters when a test point output is obtained which does not have 4 levels.

Listed below are the four test points and the particular counters associated with each.

TP107 ..... 3rd, 4th and 5th counters
TP108 ..... 5th, 6th and 7th counters
TP109 ..... 7th, 8th and 9th counters
TP110 ..... 9th, 10th and 11th counters

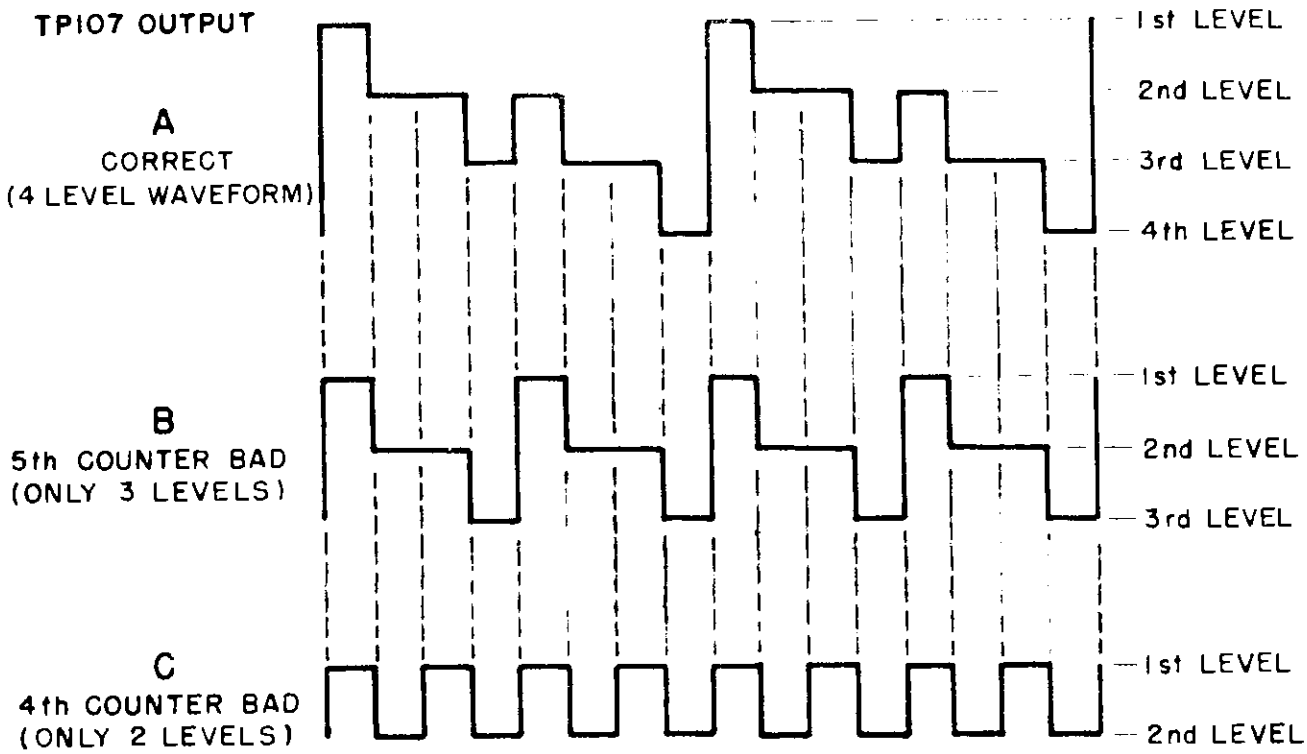


Figure 30
USE OF TP107, TP108, TP109 & TP110
TO LOCATE TUBE FAILURE

21.3 TROUBLE SHOOTING CHART FOR TIME DIFFERENCE ACCURACY

If troubles should occur in the delay system and consequently, the time difference reading becomes inaccurate, Chart II will be very useful in finding and correcting any such deficiencies.

21.4 IDENTIFICATION OF PARTS

Most of the resistors, capacitors, diodes, etc. used in the Indicator-Receiver unit are mounted on terminal boards, and as an aid in trouble shooting drawings D-175 and D-176 (found at the back of this book) should be consulted. These drawings show the seven main terminal boards of this unit and identify all parts on these boards. In addition, the voltages at all terminals are given.

21.5 TUBE VOLTAGES

Another aid in trouble shooting is Chart V which lists the voltages at the pins of all tubes found in the Indicator and Receiver.

21.6 SUMMARY

There are several important rules which must be followed in order to quickly, economically and effectively repair and maintain the LR-8803 Loran equipment. They are as follows:

1. Understand the basic principles of the Loran navigational system.

2. Understand the LR-8803 circuitry.

3. Use the proper test equipment. A TS-251/UP Loran Pulser and a good oscilloscope are absolutely imperative for the important LR-8803 alignment procedures.

4. Always follow the directions in Chart II when trouble shooting or aligning the delay system.

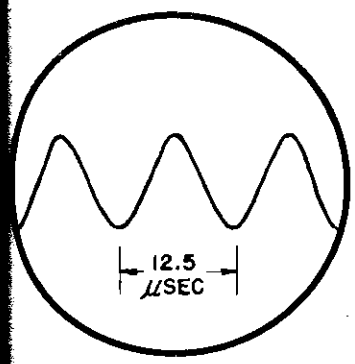
5. Never retune or adjust circuits until absolutely convinced that such a need exists.

CHART IV. TEST WAVEFORMS

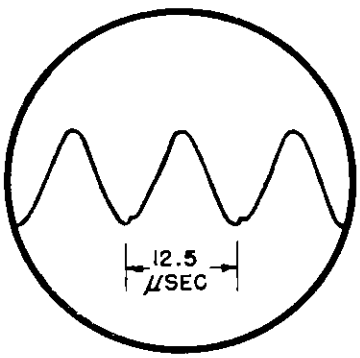
DICATOR FRONT PANEL CONTROLS SET AS FOLLOWS EXCEPT WHERE OTHER-SE INDICATED:

TE	= "HO"	TIME DIFFERENCE DIAL	= "00000 μSEC"
ANNEL	= "1"	IN AFC - OUT DRIFT	= "OUT DRIFT"
IN	= "5"	INTERFERENCE REDUCER	= "OFF"
LANCE	= "0"	LOCAL - DISTANT	= "DISTANT"
NCTION	= "1"		

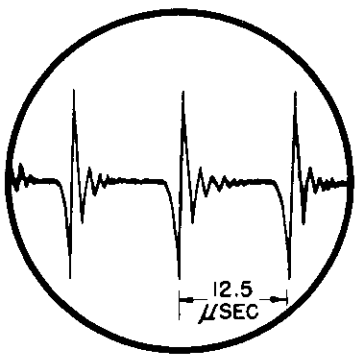
NOTES: 1. WAVEFORMS SHOW AVERAGE PEAK TO PEAK READING
2. WHEN VIEWING FULL REPITITION RATE WAVEFORMS, USE EXT SYNC FROM TP103 IF POSSIBLE



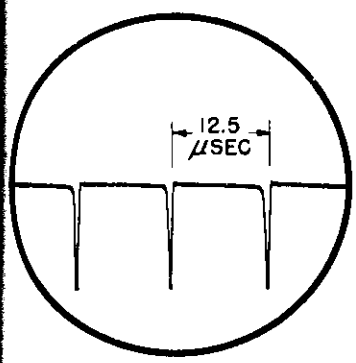
REACTANCE MOD
V101 PIN 5
125 V (APPROX) PEAK-PEAK
(P-P AMPLITUDE CHANGES SLIGHTLY WITH DRIFT KNOB SETTING)



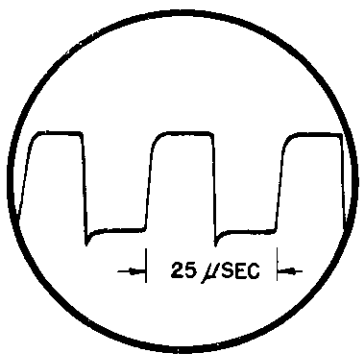
80 KC OSC
V102 PIN 1, **TP101**
100 V (APPROX) PEAK-PEAK
(P-P AMPLITUDE CHANGES SLIGHTLY WITH DRIFT KNOB SETTING)



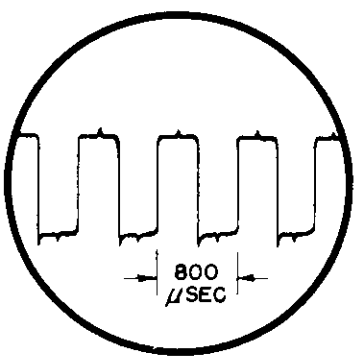
RINGER
V102 PIN 6
95 V PEAK-PEAK



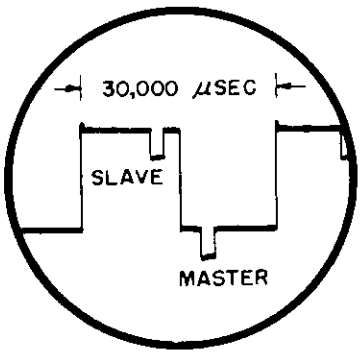
80 KC CLIPPER
V103 PIN 1
20 V PEAK-PEAK



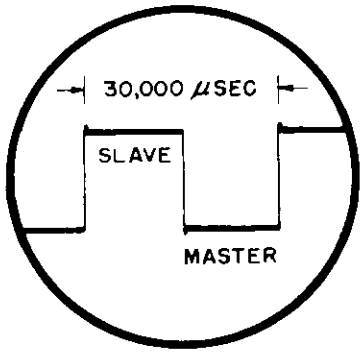
1st COUNTER
V104 PIN 6
60 V PEAK-PEAK
(VARIES WITH COUNTER BIAS SETTING)



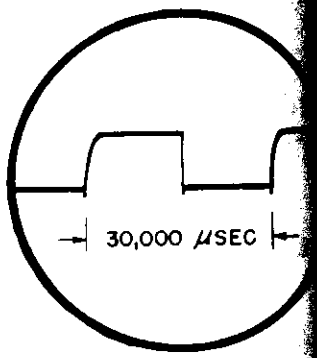
6th COUNTER
V109 PIN 6
60 V PEAK-PEAK
(VARIES WITH COUNTER BIAS SETTING)



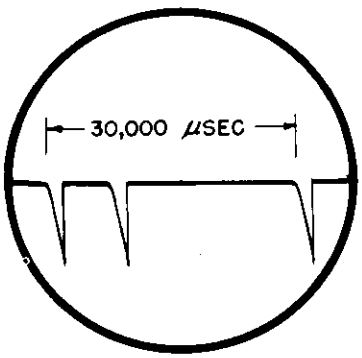
TRACE SEPARATION
S102B-3 OR C209
160 V PEAK-PEAK



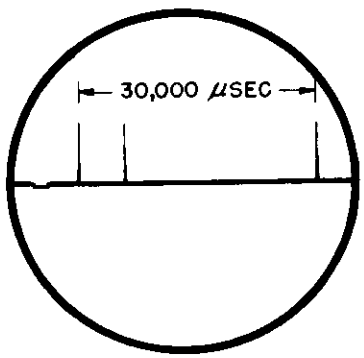
TRACE SEPARATION
S102B-3 OR C209
130 V PEAK-PEAK
(FUNCTION 2)



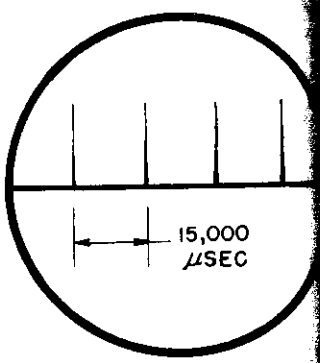
BALANCE POT
CENTER ARM
(WITH ARM AT EITHER EN
R217
10 V PEAK-PEAK



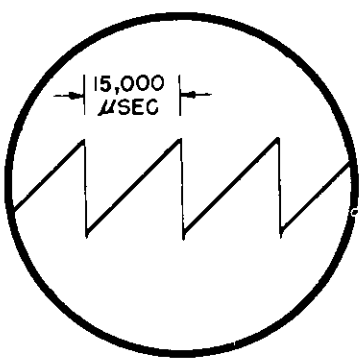
SWEEP GEN
V145 PIN 5
200 V PEAK-PEAK
(FUNCTION 2)



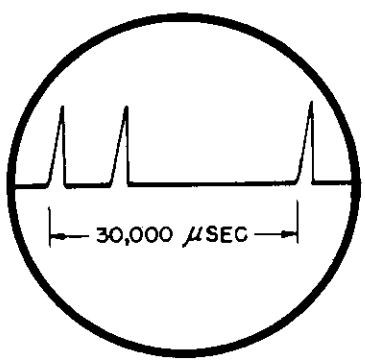
PEDESTAL GEN
V143 PIN 2
10 V PEAK-PEAK



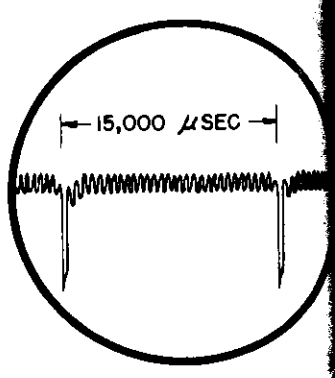
PRR RESET GEN
V116 PINS 2, 5 & 7
150 V PEAK-PEAK



SWEEP INVERTER
V144 PIN 6
150 V PEAK-PEAK



SWEEP INVERTER
V144 PIN 6
150 V PEAK-PEAK
(FUNCTION 2)



RINGER
V102 PIN 7
80 V PEAK-PEAK
(LEFT-RIGHT IN LEFT POSITI