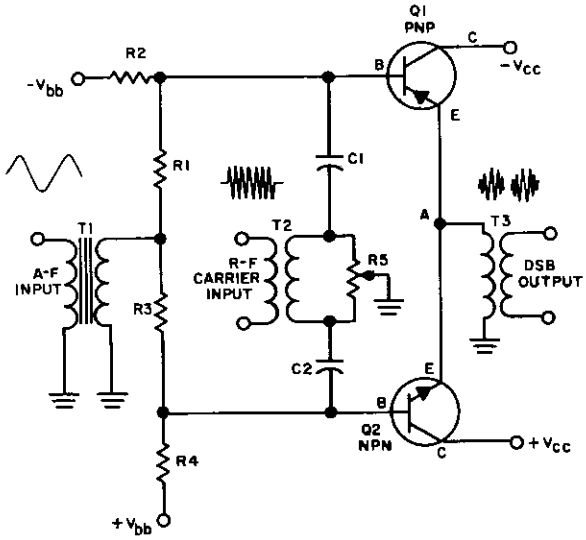
should be noted that, while the transistors are of opposite polarities, they have the same operational characteristics. The audio modulation and the r-f carrier beat together in the nonlinear resistance of the transistors, and sum and difference (sideband) frequencies are produced. The sideband frequencies are developed across the output transformer and are inductively coupled to the following stages. Circuit elements are arranged so that the r-f carrier and the original audio modulating signal do not appear in the output. For minimum distortion the r-f carrier is maintained at a level 8 to 10 times greater than the audio modulating signal.

Circuit Operation. The accompanying diagram illustrates a balanced complementary symmetry modulator.



Balanced Complementry Symmetry Modulator (common collector configuration)

Audio transformer T1 couples the audio modulation from the preceding stages to the bases of Q1 and Q2 through bias resistors R1 and R3. R1 and R2 form a voltage divider network to bias transistor Q1 and resistors R3 and R4 form a voltage divider to bias transistor Q2. Transformer T2 couples the r-f carrier from the carrier oscillator to both sides of carrier balance potentiometer R5. Carrier balance potentiometer R5, which has its slider grounded, effectively centertaps the secondary of carrier input transformer T2, causing 180° out-of-phase r-f carrier signal voltages to be present at the top and bottom of T2. Coupling capacitors C1 and C2 couple the r-f carrier from transformer T2 to the base of each transistor and prevent a DC path from being formed from the base of each transistor to ground through carrier balance potentiometer R5. Transistors Q1 and Q2 are the nonlinear devices used to generate the sidebands, and transformer T3 serves as the output load for the balanced complementry symmetry modulator.

Since both transistors have the same operational characteristics both transistors conduct equally with no signal input, and thus both transistors have equal equivalent emitter-collector resistance. Thus, it can be seen that a balanced condition exists between Q1 and Q2, and the voltage drop across Q1 is equal to the voltage drop across Q2. Since the absolute value of voltage between each power supply and ground is the same and the voltage drop across the transistors is equal, there is no voltage between point A in the figure and ground, and thus no current flows through output transformer T3, and no output is produced.

When a push-pull (180° out-of-phase) input a signal is applied, in this case the r-f carrier, the following takes place. During the period of the input cycle when the base of Q1 is driven positive and the base of Q2 is driven negative, conduction of both Q1 and Q2 decreases. This is due to a reduction in forward bias applied to each transistor (PNP transistor Q1 normally has its base biased more negative than its emitter and NPN transistor Q2 normally has it base biased more positive than its emitter). This decrease in conduction of Q1 and Q2 is in effect an increase in equivalent emitter-collector resistance and, since both transistors have the same operational characteristics, both transistors decrease conduction in equal amounts. Although the equivalent emitter-collector resistance of both transistors increases, it increases equally in both transistors and, therefore, the voltage drop across Q1 remains equal to the voltage drop across Q2. Once again the balanced condition between Q1 and Q2 is maintained and no output is produced, since no current flows through output transformer T3. During the next half-cycle of r-f carrier input a negative-going half-cycle of r-f is coupled from transformer T2 to the base of Q1 and increases the forward bias on Q1 causing the conduction of Q1 to increase. Simultaneously, a positive half-cycle of r-f is applied to the base of Q2, where it again increases the forward bias on Q2, causing the conduction of Q2 to increase. Both transistors increase conduction at the same rate, and the equivalent emitter-collector resistance of both transistors decreases equally. Again the voltage drop across each transistor is equal and a balanced state is maintained. Hence no output is produced. In this manner the r-f carrier is effectively suppressed in the complementry symmetry balanced modulator. In actual practice, the slight differences in characteristic found between evenly matched pairs of transistors necessitates the use of some external method of balancing the circuit. The complementry symmetry balanced modulator achieves precise carrier balance by making it possible to vary the amplitude of the r-f carrier coupled to the base of Q1 with respect to the amplitude of the r-f carrier coupled to the base of Q2. This is achieved by effectively center-tapping the secondary of r-f carrier input transformer T2 by connecting both sides of potentiometer R5 across the secondary of T2. Varying the position of the grounded slider of R5 has the same effect as

varying the position of the center-tap on a centertapped transformer.

When audio modulation in addition to the r-f carrier is applied simultaneously to the balanced modulator, upper and lower sidebands are generated as the result of the r-f carrier frequency and the audio modulating frequency beating together in the nonlinearly operated transistors. Four basic frequencies are present in the emitter circuit of the transistors. These frequencies are the original r-f carrier frequency, the original audio modulating frequency and the sum and difference frequencies (sidebands) resulting from heterodyning action. However, only the sideband frequencies are present in the output.

The audio modulation is applied to the base of each transistor in parallel (in phase) through transformer T1. During the positive half-cycle of modulation input the forward bias on Q1 is opposed by the modulating signal (Q1 is a PNP transistor) and conduction of Q1 decreases. At the same time, the positive half-cycle of modulating signal aids the forward bias on Q2 (Q2 is an NPN transistor) and conduction of Q2 increases. The balance between Q1 and Q2 is now upset since the equivalent emitter-collector resistance of Q1 increased causing an increased voltage drop across Q1, while the equivalent emitter collector resistance of Q2 decreased causing a decreased voltage drop across Q2. Point A in the figure is no longer at ground potential but at some positive voltage and current flows through output transformer T3 causing an output to be produced. The r-f carrier component of emitter current is cancelled as explained previously. The sideband component of emitter current and the original audio modulation component of emitter current flows through the primary of output transformer T3, but the output transformer presents a very low impedance to audio frequencies, therefore, audio frequency voltage is not developed across the primary of T3. Only the upper and lower sideband signal voltage is developed across the primary of output transformer T3 and is inductively coupled to the following stages. Overall circuit operation is the same for the negative half cycle of audio modulation input. That is, during the negative half-cycle of modulation input the forward bias on Q1 is increased and conduction of Q1 increases. At the same time, the negative half-cycle of modulation signal decreases the the forward bias on Q2 (an NPN transistor) and decreases conduction of Q2. The balance between Q1 and Q2 is now upset because the equivalent emitter-collector resistance of Q1 decreased, causing a decreased voltage drop across Q1, while the equivalent resistance of Q2 increased causing an increased voltage drop across Q2. Point A in the figure, is therefore, no longer at ground potential, but is at some negative voltage so that current flows through output transformer T3, causing an output to be produced. The r-f carrier component of emitter current is cancelled as explained previously. Although both the sideband component of emitter current and the original modulation component of emitter current both flow in the primary of T3, the low impedance offered to the audio modulation is insufficient to develop an audio frequency voltage across it. Therefore, only the upper and lower sidebands are inductively coupled to produce an output in the secondary of T3.

FAILURE ANALYSIS.

General. When making voltage checks, use a vacuum tube voltmeter to avoid the low values of multiplier resistance employed on the low voltage range of the standard 20,000 ohms-per-volt meter. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low resistance reading.

No Output. Since transistor Q1 and its associated circuit performs essentially the same function as transistor Q2 and its associated circuit components, failure of either transistor or associated circuit components is not likely to cause a no-output condition to exist. Likewise, failure of either the positive or negative power supply is not likely to cause a no-output condition to exist, since each power supply serves only one branch of the modulator. Failure of a component, such as the audio modulation input transformer T1, the r-f carrier input transformer T2, or output transformer T3 all of which serve bath branches of the modulator could be a cause of a no-output condition. Continuity checks of the transformer windings and resistance checks for shorts to ground or excessive leakage between windings will reveal a defect in either T1, T2, or T3 which could cause a no-output condition to exist. Failure of T1 or T2 could cause a no-output condition to exist by failing to couple either the audio modulation or the r-f carrier to the balanced modulator. Likewise, failure of the source of the signals (modulating signal or r-f carrier) would also create a no-output condition. To determine whether or not the signals are reaching the balanced modulator observe, with an oscilloscope, the waveform present on the primary of audio input transformer T1, and the waveform present on the primary of r-f carrier input transformer T2. Absence of either of these signals results in a no-output condition and indicates that the fault lies in the stage, or stages preceding the modulator.

Low Output. Failure of almost any component in the complementry symmetry balanced modulator could result in a decreased output. Failure of, or improper output from from either power supply could result in low output and the power supplies should be checked and repaired or adjusted, if necessary, before any component substitutions are attempted. Deterioration of either of the transistors could also be a cause of decreased output. A low output condition could also be due to improper base bias applied to either transistor. Check the voltage present on the base of Q1 and Q2 with a vacuum tube voltmeter. If a discrepancy is found the most likely cause is a change in value of voltage divider resistors R1 and R2 (for the base of Q1) or R3 and R4 (for the base of Q2). Improper base bias could also be caused by a short in coupling capacitor C1 or C2. If C1 or C2 opened, a low output condition would result since the r-f carrier would be unable to reach the base of either Q1 or Q2. A partial failure of transformers T1 or T2 could result in

decreased amplitude audio modulation, or decreased amplitude r-f carrier, reaching the bases of the transistors. This condition would likely result in decreased output. Careful resistance and leakage checks, with an ohmmeter, would usually indicate a partial failure that could be the cause of low output. Likewise, decreased amplitude r-f carrier or audio modulation before it reaches the modulator could be the cause of low output. The existance of this condition can be determined by observing, with an oscilloscope, the amplitude of the input signals on the primary of the respective input transformer. Another possible cause of low output could be due to a defect in output transformer T3. Resistance and leakage checks of the transformer windings should indicate a possible defect.

Distorted Output. Distortion of intelligence will occur in single sideband systems when the transmitter and receiver are not exactly on frequency. Distortion in single sideband transmitters is usually the result of improper operation of the linear power amplifier, or of operating any stage beyond its rated capabilities. If system distortion is determined to be caused by the modulator, almost any component which could cause low output can also be suspected of causing a distorted output. The power supply voltages should be checked first and adjusted, if necessary. A check of base bias voltage of both transistors would reveal if a fault exists in voltage divider resistors R1, R2, R3, and R4. An open or shorted carrier balance potentiometer R5 could also couse a distorted output to result. excessive audio input could be the cause of distorted Since the r-f carrier input amplitude should, for good fidelity, be 8 to 10 times the amplitude of the audio modulating signal, a decrease in amplitude of the r-f carrier or excessive audio input could be the cause of distorted output. The amplitude of the r-f carrier input and the amplitude of the audio modulation input can be easily checked by observing, with an oscilloscope, the waveform present at the primary of the respective input transformer.

Do not overlook the possibility that the audio modulating signal is distorted before it reaches the modulator.

FREQUENCY MODULATORS (FM).

The semiconductor FM modulator varies the frequency of a carrier above and below the center frequency similarly to that of the vacuum tube. Frequency modulation is usually accomplished at very low levels as compared with tube operation. In many instances the modulation is accomplished with a low-frequency carrier and the modulated carrier is then frequency multiplied until the desired center frequency is reached. Since the input and output impedances of the transistor are functions of the operating point, the transistor may be used as a reactance modulator. Thus a transistor oscillator with a tank circuit may be used with the output side of the modulator connected across part of the tank coil. Thus voice variations of the modulation signal vary the reactive output impedance of the modulator and change the oscillator frequency accordingly. Another modulation method is to vary the operating point of the modulator by varying the bias. We find then, that the modulation can be inserted in either the emitter, base, or collector circuits. Since the reactance modulator is more efficient and provides large deviation it will be discussed in the following paragraphs.

BASIC REACTANCE MODULATOR.

APPLICATION.

The reactance modulator is used to frequency modulate low power semiconductor transmitters.

CHARACTERISTICS.

Uses collector to emitter output capacitance to provide reactive frequency control.

Operates at relatively low power levels.

Shunts a portion of the oscillator tank coil.

Requires further limiting or clipping to eliminate a residual 10 to 15 percent amount of AM modulation.

Uses a single transistor to achieve full modulation.

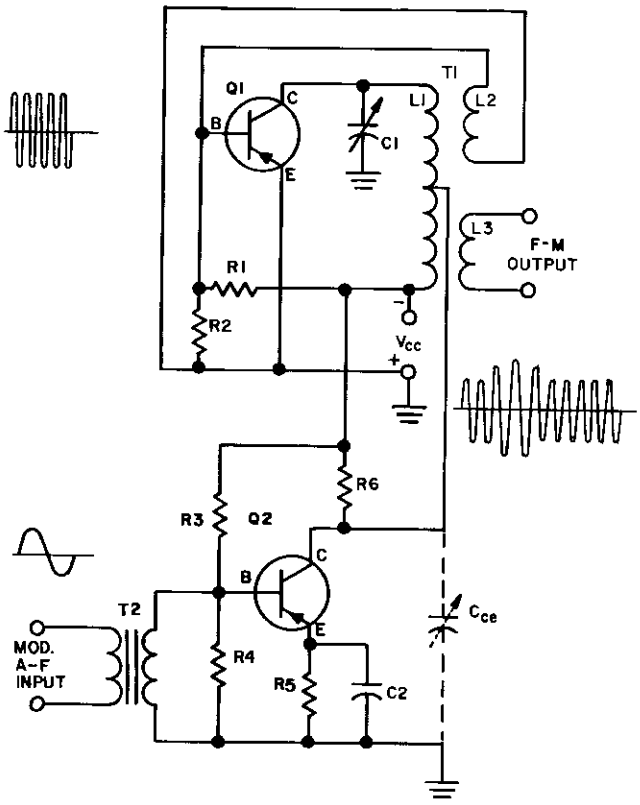
CIRCUIT ANALYSIS.

General. In an fm transistor, modulation is accomplished at the oscillator stage. The transitor oscillator is frequency modulated in the same manner as an electron tube oscillator, or by varying the gain at the modulating rate as is done with AM transistors. When the oscillator is fm modulated a slight amount of AM modulation is also inserted. Thus the modulated fm oscillator requires a limiter stage to remove the amplitude modulation before it is further amplified or multiplied in frequency. This is easily accomplished in a single stage.

Circuit Operation. The accompanying schematic shows the circuit of a typical frequency-modulated oscillator stage operated as a reactance modulator.

Transistor Q1 is the FM oscillator. Resistor R1 and R2 are base bias voltage dividers. Primary L1 of transformer T1 together with capacitor C1 form the tuned tank adjusted to the oscillator output frequency. R6 is the modulator load resistor. Secondary L2 of T1 is the collector to base feedback winding of the oscillator. Tertiary winding L3 is an inductively coupled output winding which couples the FM output signal to the next stage, or in special coses to an antenna. Transformer T2 is an audio transformer which inductively couples the modulation input to the base-emitter junction of Q2, the modulator stage. Resistors R3 and R4 are base bias voltage dividers, while R5 is an emitter swamping resistor bypassed by C2 for temperature stabilization. The output capacitance of Q2 shown dotted as Cce shunts a portion of the r-f oscillator coil L1. As the modulator operates the output capacitance of Q2 is varied. Thus, the frequency of the oscillator is shifted in accordance with the modulation the same as if C1 were varied instead.

When the modulation is applied to the primary of T2 it is coupled into the base circuit. Thus the emitter-base bias changes constantly at the modulation rate. Since the bias is increasing and decrensing at the modulating rate, the collector voltage of Q2 also increases and decreases at



Reactance Modulator

the modulating rate. When the collector voltage increases, output capacitance Cce decreases, and conversely, when the collector voltage decreases. (An increase in voltage has the effect of spreading the capacitor plates further apart by increasing the width of the PN barrier. Conversely, the reduction of collector voltage reduces the width of the PN junction and has the same effect as pushing the capacitor plates together to provide more capacitance).

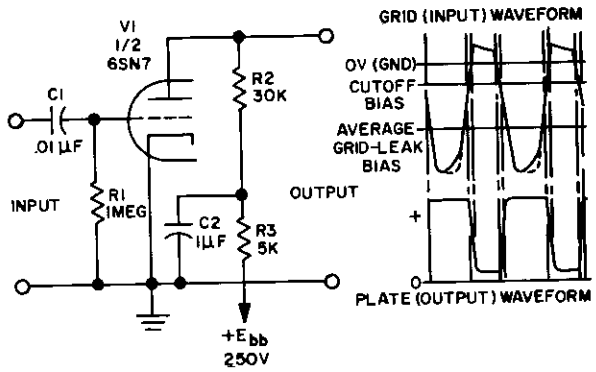
When the output capacitance of Cce decreases because of the increase in collector reverse bias, the resonant frequency of the Q1 oscillator tank circuit increases as if C1 were decreased, and produces a higher frequency r-f output. Conversely, when the output capacitance of Cce increases because of a decrease in collector reverse bias, the resonant frequency of Q1 oscillator tank circuit decreases and produces a lower frequency r-f output because of the shunting effect of Cce. Thus the resonant frequency of the oscillator tank circuit is increasing and decreasing at the modulating rate. Hence, the oscillator frequency is also increasing and decreasing at the modulation rate. The output of the oscillator, therefore, is a frequency modulated carrier signal. Since the audio modulation causes the collector voltage to increase and decrease, there is an AM component induced into the output. This produces both an FM and AM output. By placing a limiter stage after the reactance modulator, the amplitude variations are removed and only the frequency modulation remains, with a constant amplitude output. Frequency multipliers are then used to increase the oscillator frequency to the desired output frequency. For high power, linear r-f amplifiers are used to increase the steady amplitude signal to a particular level and power output. With the initial modulation occuring at low levels fm represents a saving in power as compared with conventional AM, with the FM noise reducing properties providing a better signal to noise ratio than is possible with AM.

FAILURE ANALYSIS.

General. When making voltage checks, use a vacuum-tube voltmeter to avoid the low values of shunting resistance employed on the low voltage ranges of conventional voltmeters. Be careful also to observe proper polarity when checking continuity with the ohmmeter, since a forward bias through any of the transistor junctions will cause a false low resistance reading.

No-Output. Open bias resistors, open collector resistor R6, or open windings on T1, can cause a no-output condition. Check the resistors for proper value with an ohmmeter and the transformer for continuity. If satisfactory indications are obtained but Q1 does not oscillate, the transistors may be defective. If Q1 operates but no modulation is obtained, Q2 is defective.

Low Output. Low collector voltage, low bias voltage, or a weak transistor may cause a low output. Check the supply voltage first to be certain it is normal, then check the collector voltage of both Q1 and Q2, and the base bias of Q1 and Q2 also, if the collector voltage is normal. Also check collector resistor R6 for proper value if the modulation appears weak. Low bias can be caused by a change in bias voltage dividers R1 and R2, and R3 and R4; check for proper resistance value with an ohmmeter. A high resistance connection in output winding L3 of T1 may also occur and course a reduced output.



Overdriven Amplifier Used in Radar Timing Circuitry, and Waveforms

below cutoff, until the grid voltage rises (becomes less negative) to the cutoff potential. The triode then conducts, as the grid voltage rises to zero (ground) potential. When the signal drives the grid to zero bias, grid current begins to flow, limiting any further rise of the grid voltage at this point. The grid current charges coupling capacitor C1, through the relatively low grid-to-cathode resistance of triode V1, to an average voltage which serves as a highly negative bias for the grid of triode V1. During this time the plate (output) voltage has fallen abruptly, decreasing nearly to zero, and it remains at that value until the grid signal falls, from its positive peak, back to zero. At zero bias, the plate current begins to fall rapidly as the grid voltage becomes more negative, until cutoff is reached, when the plate current has fallen to zero. During this time the plate (output) voltage has risen sharply to its maximum value of Ebb. From the waveforms shown, it should be noted that the negative portion of the output waveform is narrower than the positive portion; this is due to the fact that the tube conducts only during a portion of the positive half-cycle of the input signal, while it remains nonconductive during the entire negative half-cycle.

FAILURE ANALYSIS.

No Output. The cause of a no-output condition in the triode overdriven amplifier limiter may be defective triode tube, failure of the plate supply voltage, an open input or output coupling capacitor (if either is used), or failure of the input signal. Assuming that the tube has been determined to be capable of operation, and that an input signal of proper amplitude and polarity is present at the input to the circuit, an open plate load resistor (or plate decoupling resistor if a decoupling circuit is used) would render the circuit inoperative, and no output would be available. A shorted decoupling bypass capacitor (C2 in the second circuit illustrated), if a decoupling circuit is used, may also be the cause of a no-output condition. An open coupling capacitor in the input grid circuit, if one is used, would likewise prevent any output from being produced.

Reduced or Unstable Output. When the output of the triode overdriven amplifier becomes unstable or is of reduced value, a low value of plate voltage, due to a defective power supply, or an increased value of plate load resistance, due to a defective or "aging" resistor, may be the cause of this condition. Either a leaky input or output coupling capacitor or an open grid resistor could be responsible for unstable operation. The triode tube itself may have low cathode emission; this would produce a reduced output. Finally, the input signal itself should be checked to ascertain whether it is of correct waveform and has sufficient amplitude, since any deficiency in the input signal would be evident in the output from the overdriven amplifier.

PENTODE LIMITER.

A limiter is a circuit used to reduce, or for all practical purposes, remove the effect of unwanted amplitude variations, which occur because of inherently different levels, atmospheric disturbances, or because of unequal response of tuned circuits within a receiver, or in a combination of circuits. It restricts to a specific voltage level either the positive, the negative, or both portions of the waveform.

Two major uses for limiters are found in video circuitry and radio frequency circuitry. In video circuitry the limiter follows the video detector stage and precedes the low level, cathode-follower output stage. In this position it performs the function of both amplifying and limiting low level video signals. In the case of r-f circuitry the limiter is located after the last i-f amplifier stage and prior to the discriminator (detector) stage in an fm receiver. Here again it serves to amplify the i-f signal as well as limit it. The limiter is important in both video and r-f circuitry, since in both cases the circuitry following the limiter stage is sensitive to amplitude variations.

Limiting is accomplished by utilizing the cutoff, saturation, and grid current characteristics of an electron tube. Careful examination of the two types of vacuum tubes (triode and pentode) which are most feasible for use in limiter circuits reveals the advantages of the pentode over a triode. An important advantage is the sharp cutoff characteristic which is especially apparent in the pentode and not apparent in the triode. This characteristic permits the tube to attain cutoff with a less negative-going (smaller) signal. At the same time, the pentode has the advantage of greater electrode voltage swing. This is made available by the large range of voltages which may be applied to not only the plate of the tube (as in the case of the triode) but also the screen grid. The greater the screen voltage, the larger is the range of plate current and applied voltage. These characteristics make available a greater range over which saturation, cutoff, and grid conduction may occur.

When both plate and screen grid voltages are lowered, a smaller input signal is required to drive the plate current into saturation. At the same time, smaller negative voltage

values are also required to drive the tube to cutoff; therefore, better limiting is provided for weaker input signals when lower electrode potentials are used, rather than the full rated operating potentials.

On the other hand, by increasing electrode potentials and utilizing grid leak bias good limiting can also be obtained and, at the same time, a higher overall gain is made available.

In addition to the previous advantages, the pentode also has a higher transconductance (gain) which produces a higher signal to noise ratio. It also has a higher amplification factor and better isolation between input and output impedances, which is an advantage in almost any circuit. Thus, it is seen why a pentode is to be preferred over a triode for limiter circuitry. Typical pentode limiters of the video and r-f type are discussed in detail in the following paragraphs in this section of the Handbook.

VIDEO LIMITER.

APPLICATION.

The video limiter is used to amplify and limit to a specific amplitude low level video input signal voltages in radar and television equipment.

CHARACTERISTICS.

Constant output is obtained once the limiting level is reached. Linear amplification occurs up to limiting level.

Screen grid and plate voltages determine limiting level for a specific bias.

Best performance is obtained with sharp cutoff pentode—has rapid rise time —has little droop.

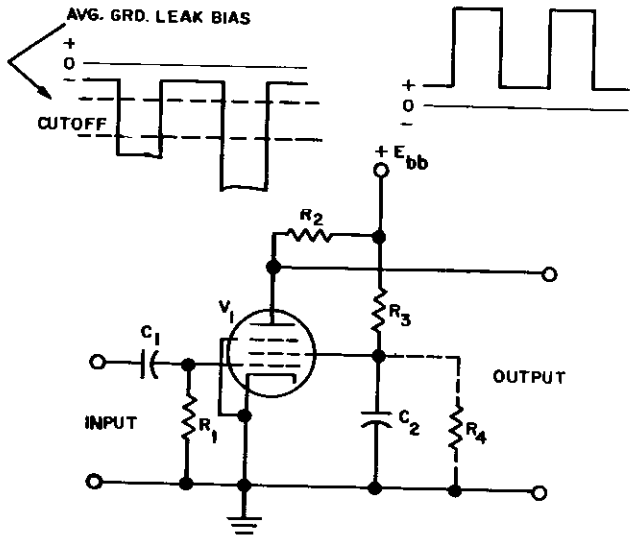
CIRCUIT ANALYSIS.

General. The pentode video limiter is located between the video detector and the low level cathode follower output stage in radar and TV receivers. Cutoff type limiting, rather than grid current or plate saturation limiting, is preferred in video limiter operation. Cutoff limiting occurs when the limiting level is determined solely by the cutoff bias level. Grid current limiting occurs when sufficient grid current is drawn to produce the desired limiting bias. Plate saturation limiting occurs when the grid bias is low or at zero and the signal drives the plate current into the saturation (no current change) level at which limiting occurs.

The limiter is supplied with a negative signal from the video detector. The signal is restricted in its negative amplitude direction by biasing the limiter tube so that cutoff occurs at the point where the desired negative voltage amplitude is attained. As the negative voltage is applied to the grid of the pentode it is inverted and amplified at the plate and coupled to the cathode follower following the limiter stage.

A pentode tube is preferred in limiter applications for several reasons. The primary reason is that the pentode inherently has sharp cutoff capabilities. This allows the tube to reach cutoff bias with a less negative-going (smaller) signal than normally would be required, and thus performs better for smaller input signals.

Circuit Operation. The schematic of a typical video limiter circuit using a pentode type of electron tube is shown in the accompanying illustration.



Pentode Video Limiter

The input signal is capacitively coupled through coupling capacitor C_1 to the grid of V_1. The combination of capacitor C_1 and grid leak resistor R_1 establish the bias potential. Plate load resistor R_2 is used to develop the plate output voltage. The screen grid dropping resistor R3 drops the screen grid voltage to the proper value and bypass capacitor C_2 places the screen at ground potential for video.

Without a signal applied, only contact bias is developed and the tube operates near zero bias. At this point the plate and screen grid voltages largely control the amount of plate current flowing.

With the application of the negative input signal (obtained from the video detector) to C_1, grid leak bias is established by the combination of C_1 and R_1. This is somewhat different than the grid leak bias explained in paragraph 2.2.2 in section 2 of this Handbook since in this application only negative pulses are used.

When the input signal used is first applied, the current through C_1 is maximum and the total input voltage is dropped across R_1, with electron flow through R_1, placing the control grid at a negative potential with respect to the cathode. C_1 charges through R_1 for the duration of the pulse. The capacitor then discharges through R_1 for the period between pulses. Before completely discharging, however, C_1 begins to charge again with the application of a new pulse. After a few cycles of operation, an average

negative voltage (bias) is established at the control grid of the tube because of the relation of the time constant of C_1 R_1 to the duty cycle of the input signal. This negative voltage (bias) establishes the cutoff point for limiting, which is determined from the plate current versus grid voltage characteristic curve of the particular pentode used for V_1. This average negative bias voltage determines where the input signal causes cutoff to occur, and thus, which portion of the input signal will be reproduced.

With the application of the input pulse, plate current flows for that portion of the pulse above cutoff. Once the tube reaches cutoff the current is at zero and remains at this point for all portions of the negative signal beyond cutoff regardless of whether or not the input signal increases. At cutoff, the plate voltage is at its maximum and, likewise, will remain at this limited amplitude for all portions of the input signal beyond cutoff. The plate voltage then decreases to a minimum value when the plate current is brought back to its maximum value by the trailing edge of the negative input pulse. Note that during the entire time the signal is less than the cutoff bias value, no limiting occurs. Thus, in the region from zero bias to cutoff, normal tube amplification action occurs. Hence, limiting occurs only for those input signals which are larger in amplitude than the value of cutoff bias. The larger the input signal, the more effective the cutoff action.

The limited voltage output level is also controlled slightly by the plate and screen grid voltages of the tube since these voltages in addition to the biasing level affect the tube characteristics and control the total amount of plate current flowing. The approximate magnitude of the limited output can be obtained from the product of load resistor R_2 and the plate current (in milliamperes) with no signal applied.

Circuit Variations. If the plate current changes between pulses because of a duty cycle change, the effective limiter output voltage is altered accordingly. This plate current change occurs if the duty ratio of the input signal is increased.

$$\text{(duty ratio} = \frac{\text{AVE. POWER}}{\text{PEAK POWER}} = \frac{\text{PULSE WIDTH}}{\text{PULSE TIME PERIOD}} = \text{duty cycle}$$

This increase in duty ratio decreases the amount of screen grid current flowing, thereby increasing the screen grid voltage. This results in greater plate current flow during the intervals between signals because of the increased voltage on the plate. An additional screen resistor R_4 placed in parallel with C_2 (as illustrated in the dotted lines in the schematic) reduces the effect of any change in plate current by voltage divider action. There will be little shift of screen voltage with increased duty ratio when the current taken by R_1 and R_2 is relatively large compared to the screen current, since the voltage division is fixed at that developed across R_2.

FAILURE ANALYSIS.

No Output. In a pentode video limiter, a no-output condition may be caused by any of the following (provided the input signal is the proper value and polarity): an open coupling capacitor C_1, an open bias resistor R_1 or plate resistor R_2, or by absence of plate or screen voltage, or by a defective tube V_1. To determine the component at fault, first check the supply voltage and then the plate and screen voltages with a high resistance voltmeter. If the supply voltage is low or zero the trouble is in the power supply or primary fuse. If the supply voltage is normal but the plate voltage is low or zerok plate load resistor R_3 may have increased in value or is open. Likewise, if the screen voltage is low or zero, screen resistor R_4 may have increased in value or is open. Check R_3 and R_4 for value with an ohmmeter. Note that zero screen voltage will also occur if screen capacitor C_2 is shorted. Meanwhile the excessive current drain through R_4 will cause it to heat, smoke, and eventually burn out. Check for a shorted C_2 by measuring the resistance to ground from the screen terminal. If both plate and screen circuits are satisfactory, check for a signal on the grid of V_1 using a vacuum tube voltmeter or an oscilloscope. If the signal appears on the grid but no output is obtained, check R_5 for proper value and continuity, since an open grid resistance will cause grid-blocking. The blocked grid will be indicated by no output and a large negative grid bias which reduces as the meter is connected from grid to ground substituting for the grid resistor. As the meter is left across the circuit unblocking will occur, and when the meter is removed the grid will again block. This indicates R_5 is either open or so large in value as to be useless. If coupling capacitor C_1 is shorted the plate voltage from the preceding stage will drive V_1 into plate current saturation. Such a condition will be indicated by obtaining identical voltage readings to ground from either side of C_1, or by checking for a short with an in-circuit capacitance checker. If all tests are normal and the trouble persists the tube is most probably at fault.

Reduced or Distorted Output. This condition may exist because: capacitor C_1 is shorted, resistor R_1 is open, screen grid bypass capacitor C_2 is shorted, plate and/or screen voltage is reduced, or tube V_1 is defective.

With C_1 shorted DC plate voltage from the previous stage will drive the grid of V_1 positive into saturation and cause a reduced output. An open R_1 will result in grid blocking and may cause audio oscillations at a slow rate. A shorted C_2 will result in reduced screen and output voltage and may also result in the burning out of resistor R_4 because of excessive screen currents. A reduced plate or screen grid voltage caused by an increase in the resistance of R_2 or R_4 will also cause reduced output voltage.

To determine the component at fault, first check the supply voltage and then plate and screen voltages with a high resistance voltmeter. If the supply voltage is low the trouble is in the power supply. If the supply voltage is

normal but the plate voltage is low, plate load resistor R_2 may have increased in value. Likewise, if the screen voltage is low screen resistor R_3 may have increased in value. Check R_2 and R_3 for value with an ohmmeter. If zero screen voltage exists screen capacitor, C_2 may be shorted. Check C_2 for shorted condition by measuring the resistance to ground from the screen terminal. If the signal appears on the grid of the tube but the output is not limited to the proper value and the electrode potentials have been checked, check R_1 for proper value with an ohmmeter. If R_1 is not within tolerance this condition will exist. If C_1 is shorted the DC plate voltage from the preceding stage will drive V_1 into plate saturation. This condition is indicated by identical voltage readings to ground from either side of C_1, or by checking for a short with an in-circuit capacitance checker. If all tests are normal and the trouble persists, the tube is most likely at fault.

R-F PENTODE LIMITER.

APPLICATION.

The r-f pentode limiter is used in f-m receivers to remove amplitude variations from the i-f signal prior to being applied to an f-m detector circuit.

CHARACTERISTICS.

Constant output is obtained once limiting level is reached. Linear amplification occurs up to limiting level.

Screen grid and plate voltage determine limiting level for specific bias.

Grid limiting and plate current saturation limiting are used in conjunction with cutoff limiting.

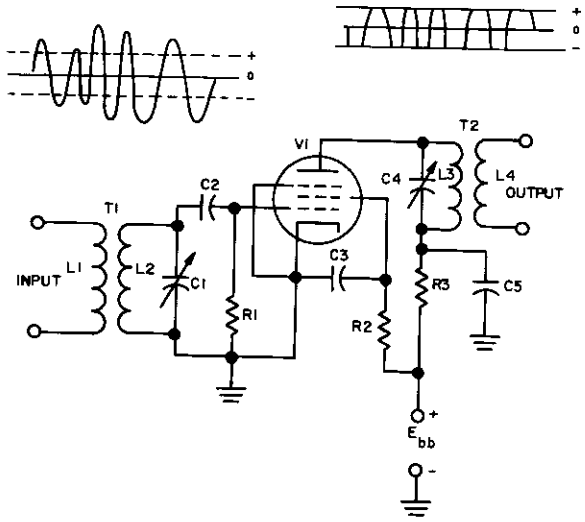
Best performance is obtained with sharp cutoff pentode-has rapid rise time-has little droop.

CIRCUIT ANALYSIS.

General. The pentode r-f limiter is located between the last i-f amplifier stage and f-m detector stage. Grid current or the plate current saturation type of limiter operation is usually used for r-f limiters. Cutoff limiting is also used with one of the aforementioned methods, but it is not used by itself, since this method can only limit the negative halves of the alternating input waveform.

The pentode, besides offering sharp cutoff characteristics, makes available a greater range of screen grid and plate voltage. Operating the plate at a low voltage produces plate current saturation, as well as plate current cutoff, more readily. In order to do this, the plate load resistor must be large enough to produce a load line below the knee of the pentode tube characteristic. Since the magnitude of the plate load resistor can not be made too large in wide-band limiter design, grid current limiting must be used where a wideband limiter is required. The effective signal voltage values that may produce current change, are those between the cutoff of the tube and the point at which grid current flow occurs or plate saturation occurs. These points, then are the limiting levels of the circuit.

Circuit Operation. A schematic of a typical r-f limiter circuit using a pentode type of electron tube is shown in the accompanying illustration.



Pentode R-F Limiter

The input signal is inductively coupled from the preceding i-f stages through primary L1 (of T1) to secondary L2, with C1 and L2 providing the proper tuning and selectivity for i-f output transformer T1. The i-f signal is then capacitively coupled to the grid of V1 through coupling capacitor C2. The combination of capacitor C2 and grid leak resistor R1 establishes the bias potential by grid current flow when a signal is applied. Plate load resistor R3 is used to drop the plate supply to the desired value of plate voltage. Screen grid dropping resistor R2 drops the supply voltage to the proper screen voltage value and bypass capacitor C3 places the screen grid at ground potential for i-f. C4 and L3 (of T2) form another tuned i-f circuit which enables the proper band of output frequencies to be inductively coupled by L4 to the f-m detector. C5 in conjunction with plate load resistor R3 forms a decoupling circuit.

When a positive-going input signal is applied to the grid of limiter V1 grid current flows, charging capacitor C2. The plate of C2 closest to the grid of V1 becomes negative and the opposite plate positive. When the signal swings negative, capacitor C2 discharges through resistor R1. The capacitor discharge current develops a voltage across R1 which makes the grid negative with respect to the cathode. When the input signal again goes positive, C2 has not had sufficient time to discharge completely. No further grid current is drawn until the input signal becomes sufficiently positive to overcome the residual negative charge remaining on capacitor C2. Each additional cycle adds a little to the charge that remains from the last cycle. After several

cycles of operation an average bias is established, and the voltage across R1 remains relatively constant. This constant voltage across R1 establishes the average bias value around which the input voltage fluctuates. This bias point is dependent on several factors, which include the vacuum tube electrode potentials, the time constant of C2 and R1 (TC=R1XC2) and the amplitude of the input signal. The last factor determines the amount of limiting performed by the grid leak bias method.

Limiting is accomplished by the instantaneous bias on the vacuum tube varying at the same rate that the peak amplitude of the input signal varies. If, on the positive portion of the signal, the peak signal amplitude increases to the point of zero bias level, or about where grid current flows, the charge on the plate of capacitor C2 closest to the grid becomes more negative with respect to the other plate. The grid bias is then increased instantaneously by the same amount to a new level and grid current no longer flows because the input level is not large enough to drive the bias to zero or above. This point is the point where limiting occurs, because in effect it is the highest positive voltage that the grid may attain. It is, thereby the value at which constant peak plate current flow occurs and the value for which minimum plate voltage is obtained.

This stable or constant (limited) plate output voltage can also be obtained by lowering the screen grid and plate voltage values to where plate current saturation, rather than grid current flow occurs, when the positive portion of the input signal reaches or exceeds the desired positive peak voltage. At this point plate current is maximum and will no longer increase with an increase in signal amplitude. Since plate current is maximum, then the plate output voltage is minimum, and remains at this limited minimum for any increase in input signal amplitude.

Although this method facilitates reaching cutoff with a less negative-going signal because of the lower electrode potentials, it is somewhat restricted by the magnitude of the plate load resistor. In order for plate saturation to occur before grid current flow, the plate load resistor value must be increased to decrease effective d-c potential at the plate. By increasing the size of the plate load resistor, however, the usable bandwidth of the limiter is lowered. Grid current limiting is therefore preferred for wide-band applications even though in order for cutoff to occur a greater negative half cycle of voltage must be present.

When the input signal is operating over the negative half-cycle, the bias is also established by the grid RC time constant, the electrode potentials, and the amplitude of the negative half cycle. If the magnitude of the negative half cycle is sufficient cutoff bias occurs. Plate current no longer flows at this cutoff point and plate voltage is at its maximum value. Thus, when the negative half cycle reaches or exceeds the cutoff bias level, plate output voltage remains at a constant limited value.

Limiting will only occur when the signal amplitude exceeds the voltage extremes necessary for grid current to flow on the positive half cycle, or (on the negative half cycle) for cutoff to occur. Any signal strength less than these amplitude extremes will result in plate current changes and plate voltage variations in accordance with this signal strength and no limiting. In order to have a constant limited output, then, the input (drive) signal strength must exceed the points where grid current flow and cutoff occurs.

FAILURE ANALYSIS.

No Output. In a pentode r-f limiter a no-output condition may be caused by any of the following (provided the signal from the previous stage is the proper value): a shorted input tank circuit capacitor C1 or output tank circuit capacitor C4, a shorted screen bypass capacitor C3, an open or shorted transformer T1 or T2, an open coupling capacitor C2, an open bias resistor R1, or by lack of plate voltage caused by an open plate resistor, R3, or a shorted plate bypass capacitor, C5, or by a defective tube V1.

To determine the components at fault, first check the supply voltage, then the plate and screen voltages with a high resistance voltmeter. If the supply voltage is normal but the plate voltage is low or zero, plate load resistor R3 may have increased in value or opened. Check R3 for value with an ohmmeter. To check if capacitors C1, C3, C4, or C5 are shorted, use an in-circuit capocitance checker. If the capacitor C2 is open or if T1 is defective, no signal would be present at the grid of V1. This may be checked by an oscilloscope. If the plate circuit is satisfactory and a signal appears at the grid of V1, but there still is no output, check resistor R1 for proper volue and continuity, since an open grid resistance will cause grid blocking. The blocked grid will be indicated by no output and a large negative grid bias which reduces as the voltmeter is connected from grid to ground substituting for the grid resistor. As the meter is left across the circuit the blocking action will subside. When the meter is removed the grid will again become blocked. This indicates that R1 is either open or so large in value that it is useless.

If T1 is open or shorted no input signal will be applied to the grid of V1. Likewise, if T2 is open or shorted no output will be obtained. Check the resistance value of the corresponding transformer primaries and secondaries with an ohmmeter (be certain to turn off the plate power before measuring). If the resistance value obtained is zero, the winding is shorted. If the value obtained is infinite, the winding is open. If all tests are normal and the trouble persists, the tube is most likely at fault.

Low or Distorted Output. This condition may exist because of capacitor C2 being shorted, capacitor C1 being open, resistor R1 being open, L1 being defective because of a partial short, or tube V1 being defective.

If C2 is shorted, d-c plate voltage from the previous stage will drive the grid of V1 positive, and into saturation, causing a reduced output. If C1 were open, i-f transformer T1 will not resonate at the proper i-f and loss of gain will result. Thus, there will be little or no output. An open resistor R1 will result in grid blocking and may cause audio oscillations at a slow rate. If screen bypass capacitor C3 is shorted, the screen and output voltages will both be reduced and eventually will result in resistor R2 burning out

because of excessive screen current. If screen bypass capacitor C3 is open, resistor R2 will have dropped across it the r-f voltage occuring at the screen grid, which will produce degeneration and result in altered screen and plate currents, and plate voltage. Reduced screen or plate voltage, caused by increased resistance of R2 or R3, will also cause a reduced output voltage. If capacitor C4 is open, the tuned circuit of L2 and C4 will not be resonant to the proper i-f frequency band. If C5 is open, the r-f voltage appearing at the plate will be fed back into the power supply through R3 and cause feedback with possible oscillation.

To determine the component at fault, first check the supply voltage and then the plate and screen voltages with a high resistance voltmeter. If the supply voltage is low the trouble is in the power supply. If the supply voltage is normal but the plate is low, plate load resistor R3 may have increased in value. Likewise, if the screen voltage is low, screen resistor R2 may have increased in value. Check R2 and R3 for proper value with an ohmmeter.

A reduced plate or screen voltage may also be caused by open capacitors C3 or C5. Check C3 and C5 with an in-circuit capacitor checker if prior checks have failed to find the fault. This same check (in-circuit capacitor checker) may be used if symptoms seem to indicate open capacitors C1 or C4. If V1 is at a constant saturation level, check C1 for a short by measuring the voltage from each plate of C1 to ground with a high resistance voltmeter, or by checking for a short with an in-circuit capacitor checker. If symptoms indicate trouble in either input or output tank circuits and capacitors C1 and C4 are not defective, remove one lead of the suspected winding and check the d-c resistance value of the winding. If all tests are normal and the trouble persists the tube is most likely at fault.

SERIES LIMITER, NEGATIVE-LOBE.

APPLICATION.

The series limiter is used in communications equipment as a speech clipper, in electronic equipment where amplitude limiting is desired (such as FM receivers or transmitters) and in waveshaping circuits where all or a portion of the negative half-cycle of a waveform is to be clipped off. This circuit is particularly suited for squaring off a peaked waveform. It is used universally in display circuits for modifying waveforms and determining the levels at which they are clipped or limited.

CHARACTERISTICS.

No amplification is realized in the circuit; because of circuit losses the output amplitude is slightly less than the input amplitude.

Positive waveform is passed unchanged, but negative waveform is either partially or completely clipped.

Phase of waveform is unchanged (output phase is same as input phase).

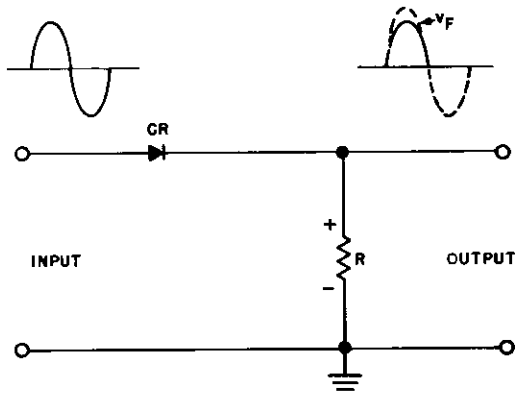
Presents a low (forward) resistance to the positive signal, and a high (reverse) resistance to a negative signal.

Isolates output circuit from input circuit in nonconducting condition.

CIRCUIT ANALYSIS.

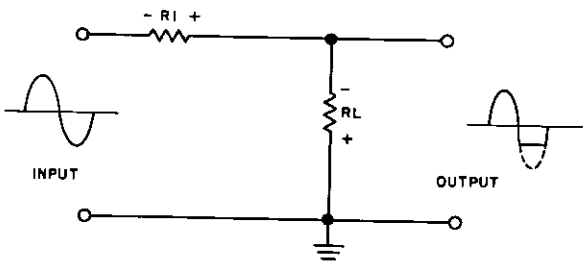
General. A limiter circuit is used to accomplish any of the following functions: to square off the peaks of an applied signal, to obtain a rectangular waveform from a sine-wave signal, to eliminate the positive or negative portion of a waveform, or to keep the input amplitude to an FM detector at a constant value. The negative-lobe limiter is designed to effectively eliminate or reduce the negative portion of the input signal.

Circuit Operation. A schematic diagram of a typical series-diode negative-lobe limiter is shown in the accompanying illustration.



Series-Diode Negative-Lobe Limiter

As can be seen, diode CR is connected in series between the input and output, with R serving as the load resistor. When a positive input is applied between the plate and ground, the cathode is made more negative than the anode, and the diode conducts. When the diode conducts, electrons flow opposite the direction of the arrow from ground, and up through R, and the polarity of the voltage developed across R is positive with respect to ground, as shown in the illustration. The amount of current flow and the resistance value determine the output voltage produced. Since the forward resistance of the diode is in series with R to ground, together they form a voltage divider and the output voltage taken across R is always less than the input voltage. (The loss (voltage drop) produced by the forward resistance is shown in dotted lines on the positive portion of the waveform and identified by the symbol V_F in the illustration). When a negative signal is applied between the cathode and ground, the cathode is made more positive than the anode, and the diode does not conduct. Thus, for this condition only the reverse resistance of the diode will allow any signal to pass to the load. Since the load resistor is not frequency-selective, the waveform of that portion of the signal produced by forward current flow through the resistor is the same as the waveform of the original signal (except where clipped) and of the same phase. The polarity, of course, is always positive. In forward conduction, the diode can be considered as a switch which connects the output to the input. Since the diode is a semiconductor, it introduces a slight amount of resistance, usually not more than 10 ohms, in series with the circuit. When the diode is nonconducting, its reverse resistance is relatively high (50K to 1 megohm, or greater), but finite (unlike the electron-tube reverse resistance which is usually infinite). In most applications, the reverse-resistance value is high enough to have little effect on circuit operation, but in a series limiter its effect may be important. The following figure shows the equivalent circuit for a diode limiter with a back resistance of 50K, plus a load resistance of 50K. As is clearly evident from the figure, the diode resistance, R1 and the load resistor, R_L, form a voltage divider across the input. Even though the diode is not conducting in the forward direction, the small leakage current which flows through the diode reverse resistance causes it to act as a voltage divider with R1. As a result half the applied input voltage appears in the output circuit. This illustrates the serious disadvantage of semiconductor limiters. As shown in the figure, the negative portion of the waveform is only partially clipped, whereas in a vacuum-tube circuit the entire negative waveform would have been eliminated. One of the practical results of this reverse-resistance effect is that diodes of one type cannot be replaced with those of another type (even though voltage and current ratings may be adequate) unless their reverse resistances are similar. Otherwise, the amount of limiting or clipping will be different from the amount selected by the designer, and improper functioning of following circuits can occur.



Reverse Resistance Equivalent Circuit

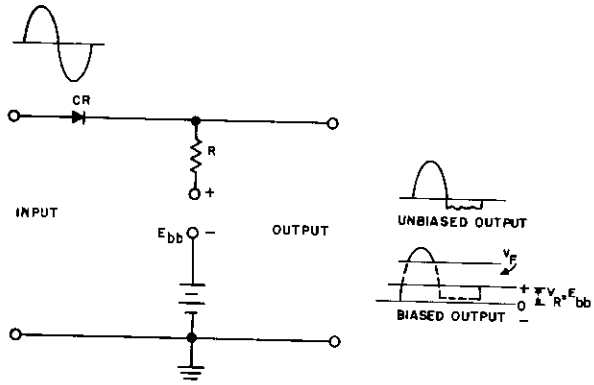
Consideration of the equivalent circuit, in the figure above, during forward resistance conditions, reveals why the output waveform can never have the same value as the input signal. If the forward diode resistance is assumed to be 5 ohms and the load resistance 50K, then the input signal will be diminished by an amount equal to the ratio of the resistance of the diode and the load and the load resistor, or one ten thousandth. It is clear from this example that the forward resistance of the semiconductor diode is low enough to produce even less loss than that of the electron tube diode, which is never less than 100 ohms and is usually more. (Practically speaking, 250 ohms is the average low value with the high value being on the order of 500 to 700 ohms).

The amount of clipping of the input waveform can be selected by using a diode which has the proper value of reverse resistance, or by placing a positive potential (E_{bb}) in series with R, as shown in the following figure. In the latter case, the diode will not conduct until the input signal is more positive than the applied bias (V_R). Thus the reverse resistance loading of the diode on the input circuit is effectively nullified (the reverse resistance voltage divider action with R is eliminated). The complete negative lobe, in this case, is eliminated. Note, however, that the voltage divider action produced by the forward resistance and R1 still remains, as indicated by v_F in the figure. The total positive signal amplitude is reduced by the amount of forward voltage drop and the effective positive bias.

FAILURE ANALYSIS.

No Output. A no-output condition can be the result of either an open-circuit condition (a defective diode, or open connection) or a short-circuit condition (R shorted). A resistance check of diode and load resistor will quickly reveal the defective component.

Low Output. Lack of sufficient input signal, as well as a defective diode, can cause a low output. A change in value of the load resistor with age, although not very likely to occur, can also cause a reduction of the output.



Bias Control of Clipping

If the diode is biased, a change of bias voltage can cause improper output. In either case, a resistance check will determine whether the components are defective, and a voltage check will determine whether the bias is correct. Be certain to observe the proper polarity when checking the diode with an ohmmeter; otherwise misleading results will be obtained.

Distortion. Except for the clipping effect, a diode limiter produces no inherent distortion. If a distorted waveform is obtained, check the input with an oscilloscope to determine whether the input signal is distorted. The positive portion of the output waveform should be identical to the positive portion of the input signal. If it is not, the diode is defective. Another possibility is that the circuit following the limiter introduces distortion by feeding back an out-of-phase signal. In some cases, it may be necessary to disconnect the limiter output to determine whether such feedback exists.

PARALLEL LIMITER, POSITIVE-LOBE.

APPLICATION.

The parallel limiter is used in communications equipment as a speech clipper, in electronic equipment where amplitude limiting is desired (such as FM receivers or transmitters) and in waveshaping circuits where all or a portion of the positive half-cycle of a waveform is to be clipped off. This circuit is particularly suited for squaring off a peaked waveform. It is used universally in display circuits for modifying waveforms and determining the levels at which they are clipped or limited.

CHARACTERISTICS.

No amplification is realized in the circuit; because of circuit losses the output amplitude is slightly less than the input amplitude.

Negative waveform is passed unchanged, but positive waveform is either partially or completely clipped.

Phase of waveform is unchanged (output phase is same as input phase).

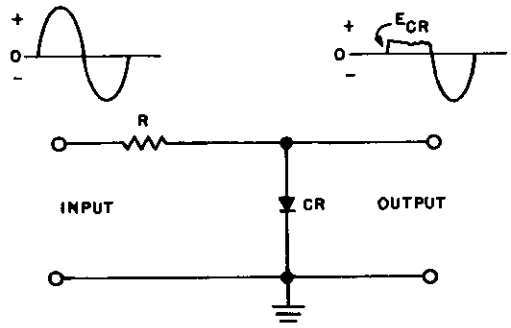
Presents a low (forward) resistance to the positive signal, and a high (reverse) resistance to a negative signal.

Output is taken from across a diode.

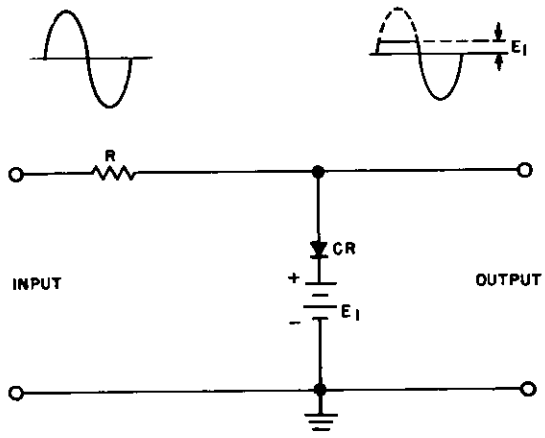
CIRCUIT ANALYSIS.

General. The positive-lobe limiter circuit is used to accomplish any of the following functions: to square off the peaks of an applied signal, to obtain a rectangular waveform from a sine-wave signal, to eliminate the positive portion of a waveform, or to keep the input amplitude to an FM detector at a constant value. The Positive-lobe limiter is designed primarily to eliminate or reduce the positive portion of the input signal.

Circuit Operation. A parallel, positive-lobe diode limiter is shown in the accompanying illustration. In this circuit, diode CR conducts only during the positive portion of the input signal. When the input signal goes positive, the diode conducts, and its resistance drops from a very high reverse resistance to a very low forward resistance. The amount of resistance of the diode in the conducting (or the nonconducting state) is determined by the internal characteristics of the particular diode selected for the circuit. Since the resistance value of R is very large compared to the conducting resistance of the diode, practically the entire value of the input voltage drops across load resistor R, while only a very small voltage drops across diode CR. This voltage may become negligible when the ratio of the load resistance R to the diode resistance is very high. Some value of voltage, however, will still exist across CR, because of its conducting resistance, called the forward resistance and is shown on the illustration as E_{CR}. When the input signal goes negative, the diode does not conduct, and current flow through R almost ceases. A small reverse current still flows through CR, because of the reverse resistance of the diode and thus a small portion of the input voltage is dropped across R. The amount of reverse resistance of the diode depends upon the characteristics of the diode selected. Thus, this is one of the disadvantages of the semiconductor diode over the vacuum tube. The vacuum tube reverse resistance is considered to be infinite, whereas the semiconductor is finite. The voltage dropped across R subtracts from the output, and thus the gain of the limiter is less than unity. On the other hand, the forward resistance of the semiconductor is less than that of the vacuum tube, making the semiconductor better in some applications.



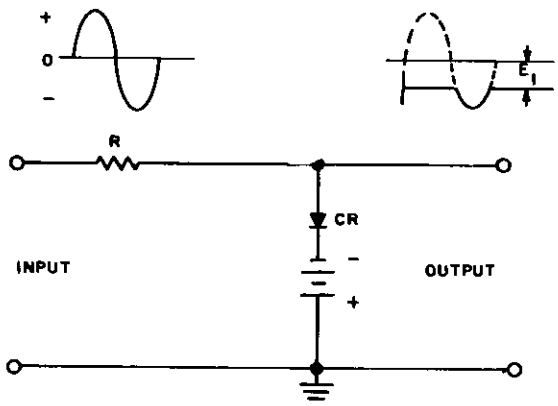
Parallel-Diode Positive-Lobe Limiter



Parallel, Positive Lobe Diode Limiter Used as a Positive Peak Limiter

A parallel, positive-lobe limiter may also be used to limit only the peaks of the positive waveform, while allowing a given value of the positive signal to pass through the circuit to the output. This may be accomplished by applying a biasing voltage, having a value equal to the value of the

positive signal to be passed by the circuit, to the cathode of the diode, as shown in the accompanying illustration. The biasing, or limiting, voltage may be obtained from a battery, as shown in the illustration, or from a tap on a bleeder resistor connected in the output circuit of a d-c power supply. When connected as shown in the illustration, with the cathode of CR connected to the positive terminal of the d-c source, the cathode of the diode is held more positive than the anode by the value of E_1 in the absence of an input signal. As long as the positive cycles of the input voltage remain less positive than E_1, the battery bias voltage, the diode remains essentially nonconducting, because its cathode is positive with respect to the anode and the output voltage is equal to the input voltage minus the voltage developed by the reverse resistance of the diode. Since all of the negative cycles of the input voltage are less positive than E_1, these too cause the diode to remain essentially nonconducting, with the result that the output voltage is again equal to the input voltage minus the voltage developed by the reverse resistance of the diode. When the input signal increases to a value which exceeds the voltage of E_1, the anode becomes positive with respect to the cathode and the diode conducts, and continues conducting as long as the input remains more positive than E_1. During this period of conduction, the output voltage of the circuit is equal to the value of E_1, and that portion of the input signal which exceeds the bias voltage is clipped, or limited, appearing as a voltage drop across the diode load resistor, R.



Parallel, Positive Lobe Diode Limiter Used to Pass Negative Peaks

By reversing the polarity of E_1, the parallel, positive lobe diode limiter may also be used where it is desired to limit not only the entire positive peaks of the input signal, but also a predetermined level of the negative peaks, in order to furnish an output only when the negative peaks exceed this predetermined level. With the cathode negative with respect to the anode, the diode is maintained in a conducting state in the absence of an input signal, and the output voltage is held at a steady (negative) d-c level equal to E_1. With an input signal applied to the circuit, the output voltage continues to be held at this steady d-c level, with the input signal appearing across the diode load resistor, R, until the input signal becomes more negative than E_1. When this point is reached, the diode no longer conducts; and its forward resistance increases to a very high value. As a result, the input signal, which previously appeared across R because R was much greater in resistance than CR, now appears across CR and the output terminals of the circuit, since CR is now much greater in resistance than R. The output signal, therefore, contains only the negative peaks of the input signal which are more negative than biasing voltage E_1.

FAILURE ANALYSIS.

No Output. A shorted diode or an open load resistor will cause a no-output condition to exist. The only other likely possibility is the absence of the input signal. Check the diode and the resistor with an ohmmeter, making certain to observe the polarities of the diode, since an erroneous indication may be obtained if the proper polarity is not observed. If both components check good, check for the presence of the input signal, making sure that it is of proper amplitude.

For the special case where the diode is not completely shorted, but reads a very low resistance of, say 200-ohms or less, the diode may be considered defective.

In the case of the biased limiter, check the bias for proper voltage with a voltmeter. In the case of a battery bias supply the voltage will be either weak or absent, but in the case of the bias supply being a power supply, it could also be high.

Reduced or Unstable Output. A defective load resistor, R, or a defect in the parallel branch of the circuit, consisting of CR and the bias supply, E_1, can produce a reduced or unstable output. The only other likely possibility is a decrease in the amplitude of the input signal. The trouble can be localized in the same manner as described above for a no-output condition.

PARALLEL LIMITER, NEGATIVE-LOBE.

APPLICATION.

The parallel, negative-lobe diode limiter is used in transistorized equipment when it is necessary to limit any part of the negative portion, or the negative going part of the positive portion of an input single waveform, and allow the remainder of the input signal to pass without modification of the waveform. It is used universally in display circuits for modifying waveforms and determining the levels at which they are clipped or limited.

CHARACTERISTICS.

No amplification is realized in the circuit; because of circuit losses the output amplitude is slightly less than the input amplitude.

Positive waveform is passed unchanged, but negative waveform is either partially or completely clipped.

Phase of waveform is unchanged (output phase is same as input phase).

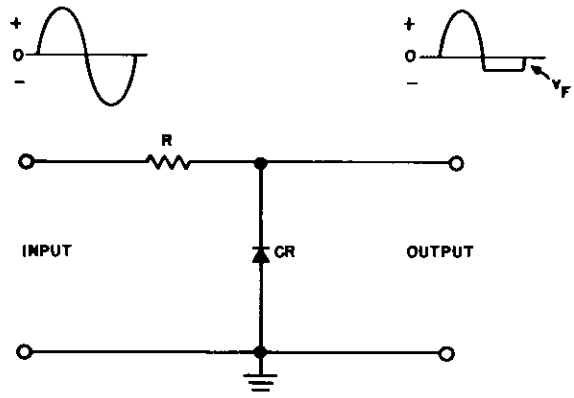
Presents a low (forward) resistance to the negative signal, and a high (reverse) resistance to a positive signal.

Output is taken from across a diode.

CIRCUIT ANALYSIS.

General. The negative-lobe limiter circuit is used to accomplish any of the following functions: To square off the peaks of an applied signal, to obtain a rectangular waveform from a sine-wave signal, to eliminate the negative portion of a waveform, or to keep the input amplitude to an FM detector at a constant value. The Negative-lobe limiter is designed primarily to eliminate or reduce the negative portion of the input signal.

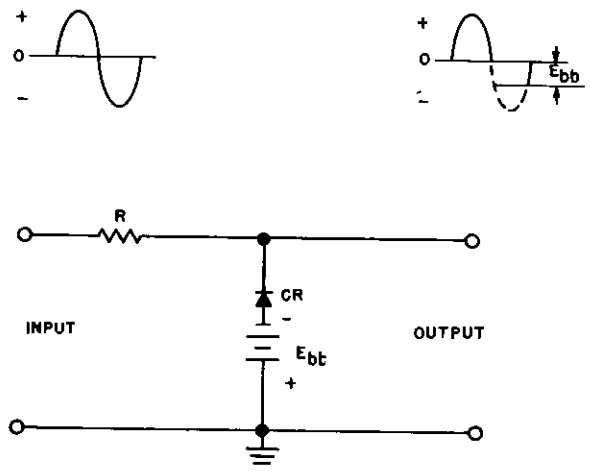
Circuit Operation. The circuit of a parallel, negative-lobe diode limiter is shown in the accompanying illustration. In this circuit, diode CR conducts only during the negative portion of the input signal. As long as the input signal remains positive, the diode remains in a nonconducting state, and current flow through R almost ceases. A small reverse current still flows through R and CR, because of the reverse resistance of the diode, and thus a small portion of the input voltage is dropped across the resistor. The amount of reverse resistance of the diode depends upon the characteristics of the diode selected. Thus, one of the disadvantages of the semiconductor diode over the vacuum tube is encountered. The vacuum tube reverse resistance is considered to be infinite, whereas the semiconductor is finite. The voltage dropped across R subtracts from the output, and thus the gain of the limiter is less than unity. On the other hand, forward resistance of the semiconductor is less than that of the vacuum tube, making the semiconductor better in some applications. When the input signal goes negative, the anode becomes positive with respect to the cathode and the diode conducts. Thus the diode resistance changes from a very high resistance to a very low resistance. The amount of resistance of the diode in the conducting state, as well as the nonconducting state is determined by the internal characteristics of the particular diode selected for the circuit. Since the resistance value of R is very large in comparison to the conduction resistance of the diode, practically the entire value of the input voltage drops across the load resistor R, while only a very small voltage drops across diode CR. This voltage may become negligable when the ratio of the load resistance R to the diode resistance is very high. Some value of voltage, however, still exists across CR, because of its conducting resistance, called the forward resistance. This voltage is shown on the illustration of the basic schematic as V_F.



Negative Lobe Diode Limiter and Input-Output Waveforms

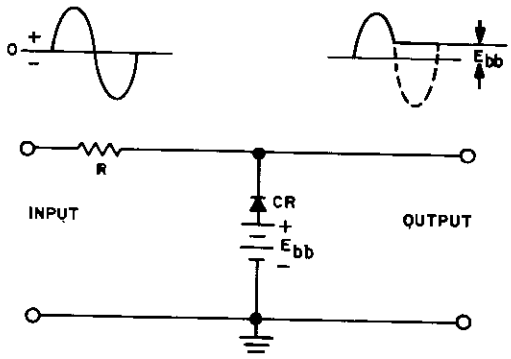
A parallel, negative-lobe diode limiter may be also used to limit only the negative waveform peak, while allowing a given value of negative signal to pass through the circuit to the output. This may be accomplished by applying a negative biasing voltage, having a value equal to the value of the negative signal to be passed by the circuit, to the anode of the diode, as shown in the accompanying illustration. The biasing, or limiting, voltage may be obtained from a battery, as shown in the illustration, or from a tap on a bleeder resistor connected in the output circuit of a d-c power supply. When connected as shown in the illustration, with the anode of CR connected to the negative terminal of the d-c source, the anode of the diode is held more negative than the cathode by the value of Ebb in the absence of an input signal. As long as the negative cycles of the input voltage remain less negative than Ebb, the bias voltage of the battery the diode remains essentially nonconducting, and the output voltage is equal to the input voltage minus the voltage dropped by the reverse resistance of the diode. Since all of the positive cycles of the input voltage are more positive than Ebb, these to cause the diode to remain essentially nonconducting, with the result that the output voltage is again equal to the input voltage minus the voltage developed by the reverse resistance of the diode. When the input signal increases to a negative value which exceeds the negative value of

long as the input remains more negative than Ebb. During this period of conduction, the output voltage of the circuit is equal to the value of Ebb, and that portion of the input signal which exceeds (is more negative) than the bias voltage is clipped, or limited, appearing as a voltage drop across the diode load resistor, R.



Parallel, Negative Lobe Diode Limiter Used as a Negative Peak Limiter

By reversing the polarity of Ebb, the parallel, negative-lobe diode limiter may also be used where it is desired to limit not only the entire negative peaks of the input signal, but also a predetermined level of the positive peaks, in order to furnish an output only when the positive peaks exceed this predetermined level. With the anode positive with respect to the cathode, the diode is maintained in a conducting state in the absence of an input signal, and the output voltage is held at a steady (positive) d-c level to equal to Ebb. With an input signal applied to the circuit, the output voltage continues to be held at this steady d-c level, with the input signal appearing across the diode load resistor, R, until the input signal becomes more positive than Ebb. When this point is reached, the diode no longer conducts; its resistance then increase to a very high value. As a result, the input signal which previously appeared across R, because R was much greater in resistance than CR, now appears across CR and the output terminals of the circuit, since CR is now much greater in resistance than R. The output signal, therefore, contains only the positive peaks of the input signal which are more positive than the biasing voltage, Ebb.



Parallel, Negative Lobe Diode Limiter Used to Pass Positive Peaks

FAILURE ANALYSIS.

No Output. A shorted diode or an open load resistor will cause a no-output condition to exist. The only other likely possibility is the absence of the input signal. Check the diode and the resistor with an ohmmeter, making certain to observe the polarities of the diode, since an erroneous indication may be obtained if the proper polarity is not observed. If both components check good, check for the presence of the input signal with a VTVM or an oscilloscope making sure that it is of proper amplitude. For the case where the diode is not completely shorted, but reads a very low resistance of say 200-ohms or less, the diode can be considered defective.

In the case of the biased limiter, check the bias for proper voltage with a voltmeter. In the case of a battery bias supply the voltage will be either weak or absent, but in the case of the bias supply being a separate power supply, it could also be high.

Reduced or Unstable Output. A defective load resistor, R, or a defect in the parallel branch of the circuit, consisting of CR and the bias supply, Ebb, can produce a reduced or unstable output. The only other likely possibility is a decrease in the amplitude of the input signal. The trouble can be localized in the same manner as described above for a no-output condition.

TWO-DIODE, POSITIVE AND NEGATIVE LOBE LIMITER

APPLICATION.

The parallel, two-diode positive and negative limiter, is used in transistorized equipment when it is necessary to limit a portion of both the positive and the negative parts of the signal waveform, and allow the remainder of the input signal to pass without modification of the waveform.

CHARACTERISTICS.

No amplification is realized in the circuit; because of circuit losses the output amplitude is slightly less than the input amplitude.

Limits a portion of both the positive and negative part of the input signal, or the entire negative or positive portion and a part of the other half, or any combination thereof.

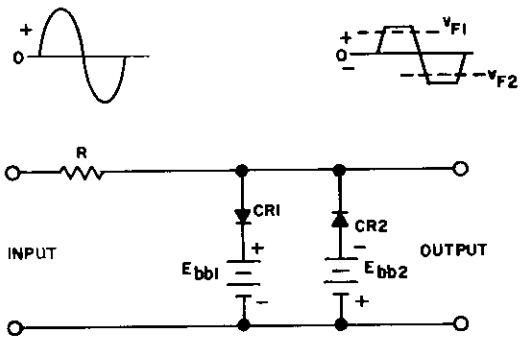
Phase of waveform is unchanged (output phase is same as input phase).

Utilizes two parallel diodes connected in opposite polarity with each other, and in shunt with the load.

CIRCUIT ANALYSIS.

General. The positive and negative lobe diode limiter is used to accomplish any of the following functions: to square off the peaks of an applied signal, to obtain a rectangular waveform from a sine-wave signal, or to eliminate the negative or positive portion of a waveform and clip the other portion. Our discussion here will primarily concern the equal clipping of both the positive and negative portions of a sine-wave, that is, the conversion of a sine-wave into essentially a square-wave.

Circuit Operation. The circuit of a parallel, positive and negative lobe diode limiter is shown in the following illustration. Diode CR1 limits the positive half cycle of the input and CR2 limits the negative half. E_{bb_1} and E_{bb_2} supply the bias for their respective diodes and the resistor, R, acts as the load resistor. Reverse biases are applied to the diodes so that the cathode of CR1 is positive with respect to its anode, and the anode of CR2 is negative with respect to its cathode.



Parallel, Positive and Negative Lobe Diode Limiter

As the signal is applied at the input and begins increasing in a positive direction, both diodes remain cut off, due to the bias, and the input signal is reproduced at the output. The output continues to follow the input signal, until a point is reached where the signal becomes more positive than the positive bias applied to the cathode of CR1. At this point, the anode becomes more positive than the cathode, and the diode conducts. When the diode conducts, it provides a low resistance path for forward current to ground, and shunts the output through the diode instead of the external load. It is at this point that the output waveform is flattened. Actually, even during its conducting period, the diode offers a slight opposition to current flow, and a small forward voltage drop adds to the load voltage. Thus, the output voltage is slightly higher than the diode bias by the amount shown as V_{F_1} on the output waveform.

As the input signal reaches its positive peak and begins decreasing towards zero, it again reaches a level which is less positive than E_{bb_1}, diode CR1 again cuts off and the input is again faithfully reproduced at the output. The input signal continues in the negative direction, and shortly becomes more negative than E_{bb_2}. When this occurs, the cathode of CR2 is made more negative than the anode, and diode CR2 conducts, duplicating the action which occured on the positive half cycle. The forward voltage drop of the conducting diode is shown as V_{F_2} on the output waveform. The input then reaches the negative peak and begins decreasing towards zero. As it becomes less negative than E_{bb_2}, CR2 ceases conducting, and the remainder of the input signal is reproduced at the output.

The amount of clipping which takes place at the output is dependent to a certain extent upon the type of diodes selected, but primarily upon the value of the bias. As E_{bb_1} is made more positive, less clipping occurs on the positive half cycle, and as it is made less positive, more clipping occurs. By the same token, as E_{bb_2} is made less positive, more clipping occurs. By the same token, as E_{bb_2} is made more negative less clipping occurs on the negative half cycle, and as it becomes less negative, more clipping occurs.

FAILURE ANALYSIS.

No Output. An open load resistor R, or the absence of the input signal are the two most probable causes of a no-output condition. Check the value of R with an ohmmeter for proper value, and check for the presence of the input signal with an oscilloscope. Note that for the diodes to produce a no-output condition, both of them must be shorted, and that the loss of both bias supplies will produce an extremely low clipped output, caused by the voltage drops across the diodes.

Low or Distorted Output. Under most circumstances, the output will be either distorted or lost completely. Distortion may be caused by a change in the bias supply, by an open or shorted diode, or distortion of the input signal. Check both bias supplies for proper voltage with a voltmeter, and both diodes with an ohmmeter. Be sure to observe proper polarities when checking the diodes, as incorrect indications could be obtained by not doing so. The input signal should be checked with an oscilloscope to determine if the input waveform is at fault.

The possibility of both half cycles of the output being decreased by the same amount is unlikely. Both bias supplies must decrease by the same amount to cause this condition. If both supplies increase, the output will increase. The only other cause of decreased output is the load resistor increasing in value.

TRIODE, BASIC COMMON-BASE LIMITER.

APPLICATION.

A triode, basic common-base limiter is used in semiconductor circuits when it is desired to limit the amplitude of a relatively small input signal to a definite negative and positive output level.

CHARACTERISTICS.

Cutoff and plate saturation limiting are used by this limiter.

Base to emitter bias and base to collector bias values determine the proper limiting level.

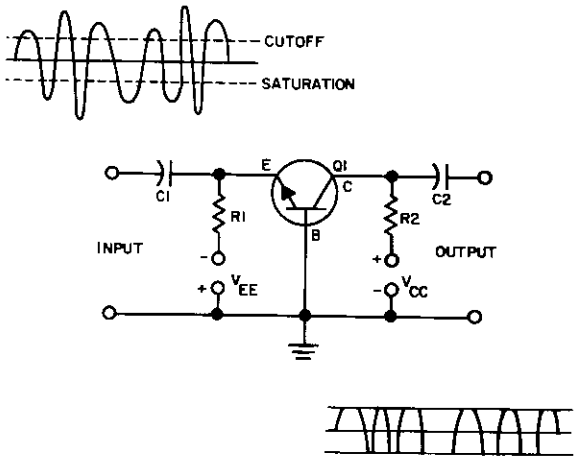
Low input impedance and high output impedance.

No phase inversion.

CIRCUIT ANALYSIS.

General. The triode, basic common-base limiter is essentially a transistor amplifier which is operated at a level which allows it to be cutoff and saturated at certain positive and negative amplitudes of the input signal. By using a specific emitter to base voltage a specific emitter current is obtained. This emitter current determines what signal level is required to cutoff and saturate the limiter. These cutoff and saturation values are the limiting levels.

Circuit Operation. A triode, basic NPN common-base limiter is shown in the accompanying illustration.



Triode, Basic Common Base Limiter (NPN)

Capacitor C1 and resistor R1 form a coupling network which couples the signal from the previous stage to the emitter of Q1. Bias supply VEE determines the emitter to base bias voltage. The value of base resistor R1 in conjunction with the bias supplied by VEE determines the emitter current. Collector load resistor R2 and collector supply VCC establish the collector current. Capacitor C2 couples the output of Q1 to the following stage. Q1 is an NPN transistor.

When the incoming signal is positive-going the positive signal voltage opposes the normal forward negative bias between the emitter and the base. This reduces the current flowing through the transistor. When the collector current of Q1 is reduced, the voltage drop across R2 is also reduced, and the collector voltage approaches that of the collector supply which, in effect, makes the collector more positive. Thus, for a positive incoming signal a positive output voltage is obtained.

When the positive incoming signal becomes sufficiently large that it cancels the forward bias entirely the transistor cuts off and collector current ceases. The collector voltage of Q1 is now at the supply value and cannot increase further. Hence, for any further positive increase in signal voltage there is no change in output voltage, which stays constant for any variation of input signal voltage beyond the cut-off level.

When the incoming signal is negative-going the emitter is driven negative with respect to the base. This increases the forward bias and current flow (electron flow) from emitter to collector. An increase in voltage drop across collector resistor R2 results, which drives the collector more negative. Thus, a negative input results in a negative output.

If the incoming signal exceeds a certain negative value, the current from emitter to collector reaches its maximum (saturation) value and the collector voltage reaches a minimum value. Any further increase in amplitude of the negative input signal does not affect the collector current or the voltage at the collector, since the transistor has attained a saturated level.

It is at these levels of saturation and cutoff that the output voltage is limited. Thus, to achieve limiting it is necessary to supply a large amplitude signal. Between the limits of cutoff and saturation the circuit will act as a conventional amplifier. Beyond these limits the peaks are cut off and the waveform is effectively "squared off".

FAILURE ANALYSIS.

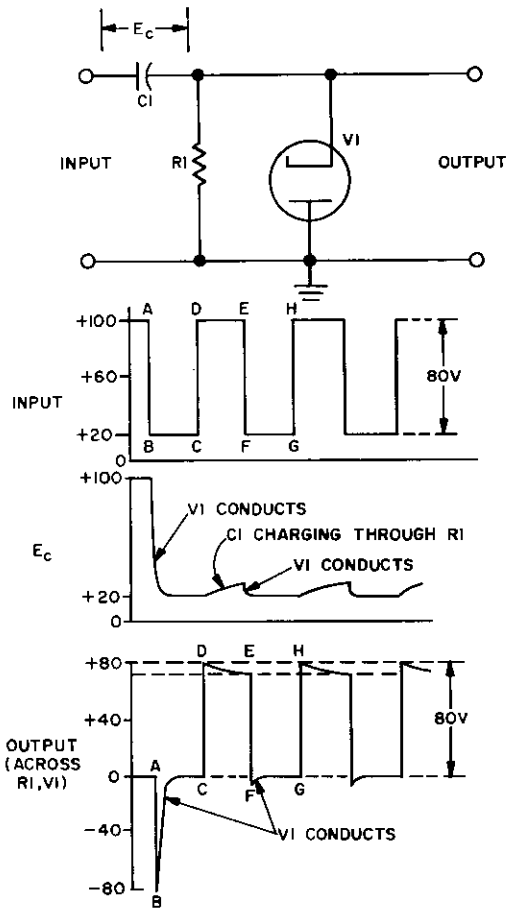
No Output. In a triode, basic common-base limiter a no-output condition may be caused by any of the following (provided the input signal is present and correct): An open coupling capacitor C1, an open bias resistor R1, an open or shorted supply voltage VEE, an open collector to base resistor R2, an open or shorted supply voltage VCC, an open output coupling capacitor C2, or a faulty transistor Q1.

To determine which of these components is at fault first use an oscilloscope to determine if the input signal is present at the input terminals of the circuit. Then determine if the input signal is present at the emitter of the transistor. If the signal is present at the input terminals but not at the emitter, first check C1 with an in-circuit capacitor checker. If C1 is not open check R1 with an ohmmeter (after disconnecting one end of the resistor from the circuit). If R1 is not open, check bias voltage VEE by either replacing it with an equivalent voltage source which is

known to be good, or by measuring VEE with a high resistance voltmeter. If VEE is not zero or shorted, check R2 with an ohmmeter (after disconnecting one end of the resistor from the circuit). If R2 is not open, check the collector bias voltage VCC with a high resistance voltmeter. Check C2 with an in-circuit capacitor checker. If C2 is not open and all other components check out, transistor Q1 must be at fault.

Low or Distorted Out. A low or distorted output may be caused by: input capacitor C1 being shorted, resistor R1 being shorted or beyond tolerance, voltage source VEE being other than the required voltage, resistor R2 being shorted or beyond tolerance, voltage source VCC being other than the required voltage, capacitor C2 being shorted, and transistor Q1 being defective.

To determine which of these components is at fault, first check the voltage between one plate of C1 and ground with a high resistance voltmeter, then check the voltage between the other plate of C1 and ground. If these voltage values are equal then capacitor C1 is shorted. Check the value of R1 with an ohmmeter (after first disconnecting one end of R1 from the circuit) for the proper ohmic value. If R1 is not within the required tolerance replace it with a resistor that is. Check voltage source VEE with a high resistance voltmeter. If the voltage has altered from the required voltage, either adjust the source to the proper value or replace VEE with a voltage source of the proper value. Check the value of R2 with an ohmmeter (after first disconnecting one side of R2 from the circuit) for the proper ohmic value. If R2 is not within the required tolerance, replace it with a resistor that is. Check voltage source VCC with a high resistance voltmeter. If the voltage has altered from the required voltage, either adjust the source to the proper value or replace VCC with a voltage source that is the proper value. Check the voltage between one plate of C2 and ground with a high resistance voltmeter, then check the voltage between the other plate of C2 and ground. If these voltages are equal capacitor C2 is shorted. If all of these components are good and the trouble still persists the fault must be in transistor Q1.



Positive Diode Clamper Circuit and Waveforms

the input waveform. Once again the charge existing on capacitor C1 cannot change immediately, and the 80-volt change appears across resistor R1. However, an 80-volt change causes the output voltage to overshoot and drop below the zero reference level slightly because of a slight charge of capacitor C1 which has occurred during the time interval between points D and E. Therefore, because of the voltage overshoot, a small negative voltage exists across resistor R1 and diode V1. The cathode of the diode is negative with respect to its plate, and the diode conducts momentarily to discharge capacitor C1. The output quickly rises and remains at zero (reference level) until point G is reached. The input signal again rises (from +20 volts to +100 volts), and an 80-volt increase in signal voltage appears across resistor R1, again causing the output to rise from zero to +80 volts. Thus, between points G and H on the waveforms, the input voltage rises from +20 to +100 volts, and the output voltage rises from zero to +80 volts. Once again, capacitor C1 begins to charge through resistor R1 to complete another cycle.

The output waveform has purposely been drawn to show a substantial decrease in voltage caused by the charging of capacitor C1 during the time the input waveform is at its positive extreme (point D to point E). In practice, however, the value of resistor R1 is relatively large, and very little distortion results from the charging of capacitor C1 through R1, or from its discharging through diode V1 (at paint F).

From the explanation of the positive clamper operation given above, it is seen that the negative extreme of the input waveform has been held, or clamped, to the desired zero reference level and the entire waveform has been shifted positively with respect to the reference level.

FAILURE ANALYSIS.

General. Because of the relative simplicity of the positive diode clamper circuit, the failure analysis is also relatively simple and is limited to several possible failures.

Initially, the input signal should be checked to determine whether it is present and of the correct waveshape and amplitude. The diode, V1, should be checked to determine whether it is in satisfactory condition and whether the correct filament (heater) voltage is applied to the tube. In many cases, a d-c potential exists at the input to the clamper circuit; therefore, it is possible for coupling capacitor C1 to become leaky (or shorted) and cause a voltage-divider action to occur. Since capacitor C1 is in series with resistor R1, a continuous current flow can result if the capacitor is leaky (or shorted), and this will produce a change in the reference level at the output of the clamper circuit. A quick check to determine whether coupling capacitor C1 is leaky (or shorted) is to remove diode V1 from the circuit and check for the presence of voltage developed across resistor R1.

If the value of resistor R1 increases considerably above its original value, distortion of the output waveform is likely to occur, especially when the input waveform is subject to changes in signal amplitude. As a result, distortion will occur during the time required for capacitor C1 to reach a new reference level, which results from a change in signal amplitude. If the value of resistor R1 decreases considerably, distortion of the output waveform will occur because of the decreased R-C time constant, and, as a result, undesirable spikes will be present in the output waveform.

Since only three components are involved in the circuit (resistor R1, capacitor C1, and diode V1), these components are easily checked to determine whether they are defective: resistor R1 can be measured with an ohmmeter to determine its resistance, capacitor C1 can be checked with a suitable capacitance analyzer, and diode V1 can be checked in a tube tester or, as an alternative, a diode known to be good can be substituted and the operation of the circuit noted.

NEGATIVE-BIASED DIODE CLAMPER.

APPLICATION.

The negative-biased diode clamper is used when it is desired to shift and hold the reference level (negative extreme for positive diode clamper, or positive extreme for negative diode clamper) of the applied signal to some negative value.

CHARACTERISTICS.

Establishes a d-c reference level of a signal, but does not affect its amplitude.

The reference level is always a negative value equal to the bias voltage.

Input and output voltages are in phase.

Uses a diode, an r-c network, and a bias voltage supply.

A negative-biased diode clamper may be used as either a positive or negative clamper.

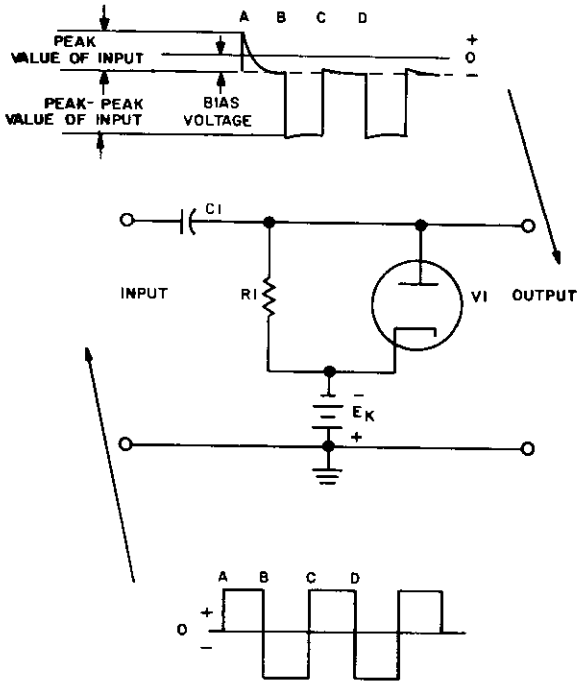
CIRCUIT ANALYSIS.

General. A diode clamper (positive or negative) is connected so that whenever the signal swings in one direction (positive direction for negative clamping—negative direction for positive clamping) diode V1 conducts to produce a short r-c time constant; whenever the signal swings in the opposite direction diode V1 does not conduct, and this results in a time constant dependent on a resistor in parallel with the diode and coupling capacitor C1, which is long with respect to the time constant of the resistance of the diode and the coupling capacitor. Thus, two different time constants are produced; a short time constant when V1 is conducting and a long time constant when V1 is not conducting.

The output voltage is obtained across the parallel combination of the diode and the resistor. During the short time constant all of the input signal voltage is developed across the coupling capacitor and none is developed across the diode and resistor, and thus no output is developed. During the long time constant, practically none of the signal voltage is developed across the coupling capacitor and practically all of the signal voltage is developed across the resistor and diode, and thus practically all of the signal appears at the output.

The clamping level is dependent on the input voltage value; normally the clamping occurs at a zero voltage reference level and extends in a positive or negative voltage direction to a voltage value equal to the peak to peak input voltage. With the insertion of a negative bias voltage the reference level is shifted in a negative direction. A negative or positive diode clamper having a negative bias will have the minimum negative voltage of the output at a reference level equal to the value of the bias voltage.

Circuit Operation. A negatively biased negative diode clamper is shown in the accompanying illustration. Capacitor C1 and resistor R1 form an r-c coupling network and determine the long time constant associated with the circuit. Electron tube V1 is an indirectly heated cathode type of diode. This diode during the time of its conduction, shunts R1 and together with capacitor C1 determines the short time constant of the circuit. Voltage source EK provides a negative bias voltage which alters the reference level from zero to a negative reference level equal to the bias potential.



Negatively Biased Diode Clamper

The input waveform shown in the accompanying illustration is a typical square wave. Prior to point A on the signal voltage waveform there is no input voltage. Prior to point A on the output voltage waveform, the output voltage is maintained at the bias voltage value. At point A the first leading edge of the input square wave occurs. Since C1 cannot instantaneously charge to this value, the full signal voltage appears on the plate of V1. The output voltage at point A is the algebraic addition of the voltage across V1 and the negative bias voltage. Capacitor C1 charges rapidly, however, because of the very small time constant (with respect to the frequency of the input signal) of C1 and the small resistance of V1 during its conduction. The output voltage diminishes to the bias voltage at the same rate that C1 charges. This voltage diminishes well before point B is reached. Then the input signal reaches point B, capacitor C1 again cannot change its charge instantaneously, and a high negative voltage appears on the plate of V1. Therefore, diode V1 does not conduct and all the voltage appears across R1. The output voltage at

point B is the algebraic sum of the negative voltage across R1 and the negative bias voltage.

During the pulse period between points B and C, capacitor C1 discharges slightly through R1 for the duration of the negative pulse. Since the time constant of R1 and C1 is large, however, only a slight amount of this voltage leaks off. The amount of the voltage that discharges through R1 subtracts from the voltage originally applied across R1 at point B. Hence, at point C the initial negative charge is less than at point B, accounting for the dip in the waveform.

When point C is reached and the input signal rises in a positive direction V1 conducts, and capacitor C1 again cannot respond instantaneously to the rapid change. Hence the full voltage appears across the diode. The output voltage this time, however, is not only the voltage across V1 plus the bias voltage but it is this algebraic addition minus the voltage that is present across R1. Since the voltage across R1 has been reduced by the discharge of C1, the voltage across R1 is less than the voltage across V1 by the amount of voltage that has leaked off C1 at point C. The output voltage at point C is then slightly more positive than the bias. This produces the slight positive peak on the waveform at paint C, since the anode of V1 is more positive than the cathode, V1 conducts and quickly charges, removing the small pip caused by the initial surge across V1. The output voltage then drops to that of the bias voltage for the remainder of the pulse width, period C to D on the waveform. When point D is reached the action is the same as that occuring at paint B and the cycle repeats.

By reversing the diode in the illustrated circuit, the circuit becomes a negatively-biased positive diode clamper. The positive diode clamper normally has a positive output with a zero reference level. By inserting the negative bias, the reference is shifted to a negative voltage value equal to the bias voltage.

FAILURE ANALYSIS.

General. Because of the relative simplicity of the negatively biased negative or positive diode clamper circuit, the failure analysis is limited to several possible failures. Before checking for failures within the clamper circuit, check the input signal to determine whether it is present and of correct waveshape and amplitude. If the signal is present and correct, the fault must exist in the clamping circuit. In many cases, a d-c potential exists at the input of the clamper circuit; therefore, it is possible for coupling capacitor C1 to become leaky (or shorted) and cause a voltage divider action to occur. Since capacitor C1 is connected in series with resistor R1 a continuous current flow can result if the capacitor is leaky (or shorted), and this will produce a change in the reference level at the output of the clamper circuit. Furthermore, in this case it is likely that diode V1 will conduct at all times. Check coupling capacitor C1 for leakage.

If the bias supply were to open, no output would be obtained. If the bias supply voltage became shorted, an output would exist, but the reference level would be shifted to zero instead of some negative value.

If the resistor R1 increases considerably above its original value, distortion of the output waveform is likely to occur, especially when the input signal is subject to changes in amplitude. If the resistor R1 decreases considerably, distortion of the output waveform will occur because of the decreased r-c time constant, and, as a result, undesirable spikes will be present in the output waveform.

Since there are only four components in the circuit there should be little difficulty in determining the faulty component. Resistor R1 may be measured with an ohmmeter to determine if its value is within the acceptable tolerance. Capacitor C1 may be checked with a capacitor analyzer or by measuring the voltage from one plate of C1 to ground and then the other plate of C1 to ground (if the voltages measured are equal the capacitor is shorted). Bias voltage source Ek may be checked with a voltmeter. If after all known good bias supply, or with a voltmeter. If after all the components have been checked the trouble still persists, diode V1 must be at fault. A low reverse resistance is also an indication of a defective diode.

POSITIVE-BIASED DIODE CLAMPER.

APPLICATION.

The positive-biased diode clamper is used when it is desired to shift the reference level of the applied signal in a positive direction. This type of circuit is commonly used in radar, television, and computers.

CHARACTERISTICS.

Output waveform varies between the positive reference level and a voltage equal to the sum of, or the difference between, the peak to peak amplitude and the positive reference voltage.

Establishes a d-c reference level for the waveform, but does not affect its amplitude.

Input and output voltages are in phase.

Uses a diode, an r-c network, and a bias supply.

A positive bias may be used with both positive and negative clampers.

CIRCUIT ANALYSIS.

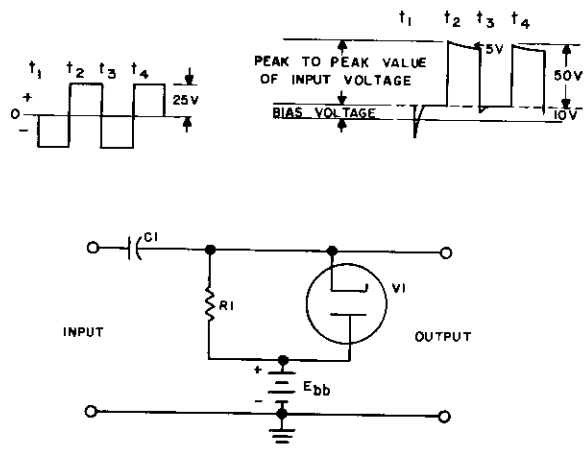
General. A diode clamper (of either positive or negative type) is connected so that whenever the waveform swings in one direction (positive direction for negative clamping and negative direction for positive clamping) the diode conducts to produce a short r-c time constant; whenever the waveform swings in the opposite direction the diode does not conduct, and this results in a time constant dependent on the r-c network which is very long with respect to the short time constant formed by diode V1 and capacitor C1.

The output voltage is taken across the parallel combination of the diode and the resistor to ground. During the short time constant, all of the signal voltage appears

across the coupling capacitor and no voltage appears across the diode, or the resistor, and thus no voltage appears at the output. During the long time constant practically none of the signal voltage appears across the coupling capacitor and practically all of the signal voltage appears across the resistor, and thus practically all of the signal appears at the output.

The clamping level is dependent upon the input voltage value, normally being clamped at a zero voltage reference level and extending in a positive or negative voltage direction to a voltage value equal to the peak to peak input voltage. With the insertion of a positive bias voltage the reference level is shifted in a positive direction. A positive diode clamper (biased positive) will have its lowest positive value as the reference level. A negative diode clamper (biased positive) will have its highest positive value as the reference level. The reference level will be, in any case, a value equal to the value of the bias voltage.

Circuit Operation. A positively biased positive diode clamper is shown in the accompanying illustration.



Basic Biased-Positive Diode Clamper

Capacitor C1 and resistor R1 form an r-c coupling network and determine the long time constant associated with the circuit. Electron tube V1 is an indirectly heated cathode-type of diode. This diode, during the time of its conduction shunts R1, and together with C1 determines the short time constant associated with the circuit. Voltage source Ebb provides a bias voltage which changes the reference level from zero to a positive level equal to the bias potential. The illustrated input waveform is a typical square wave with times t_1, t_2, t_3 and t_4 occurring at the leading and trailing edges of the waveform where the signal changes from positive to negative levels and vice versa. Prior to application of the input voltage at time t_0 the output voltage is maintained at the positive bias voltage level, that is at, say +10 volts. At time t_1, the negative-going leading edge of the square wave input pulse occurs. Since coupling capacitor C1 cannot change its charge instantly the total input voltage appears across resistor R1, and produces a negative spike of output voltage. Since V1's cathode is now driven negative with respect to the anode, diode V1 conducts. The amplitdue of the output signal at this instant is a -25 volt peak of input voltage plus a positive 10 volts bias, which add algebraically to an effective -15 volts output amplitude. When V1 conducts, the short time constant quickly discharges C1 and the negative spike drops to the bias level remaining at this value for the remainder of the pluse width. In this instance the effective zero level is not zero but is the positive bias level. Meanwhile, diode V1 is conducting lightly because of the positive bias, and creating the flat (bottom) portion of the output pulse for the time remaining between t_1 and t_2. At time t_2, the input waveform becomes positive-going and swings to the full 50 volt peak value. Again C1 cannot change its charge instantly, so the full voltage appears across R1. The output voltage now rises to +60-volts, the sum of the peak input voltage (+50) and the bias (+10). During this time the cathode of V1 is now more positive than the anode and conduction ceases. During the period between t_2 and t_3, C1 charges slowly through the long time constant supplied by R1. At time t_3 the second input pulse ends and the negative-going trailing edge causes the output voltage to drop 50 volts. Because of the small charge through the long time constant circuit, this voltage overshoots the bias level, and drops to +5 volts instead of the normal bias value of +10 volts. This occurs because capacitor C1 is charged 5-volts during the pulse width because of the long time constant. Hence, although the initial output voltage is 60 volts at time t_2, it drops to 55 volts by time t_3, due to the charging of C1. Therefore, when the negative 50 volt swing occurs at t_3, the output level drops to +5 volts. Thus an effective 5-volt negative overshoot is produced at the bottom of the waveform. The negative overshoot drives diode V1 into conduction which quickly discharges C1 to the bias level and eliminates the overshoot pip. The output now remains at the +10 bias level for the remainder of the flat (bottom) portion of the waveform. At time t_4 the waveform again changes direction and a positive-going signal is applied. The cycle now repeats, and thus the negative portion of the waveform is held clamped to the positive bias level for the duration of the input signal. The distortion shown in the illustration of the waveform is exaggerated to facilitate the understanding of circuit action. In practice, the time constant of C1 and R1 is sufficiently large that very little distortion of the waveform occurs.

By reversing the diode in the illustrated circuit, the circuit now becomes a positively biased negative diode clamper. The negative diode clamper normally has a negative output with a zero reference level. By inserting the positive bias the reference level is shifted to a positive voltage value equal to the bias voltage.

FAILURE ANALYSIS.

General. Because of the relative simplicity of the positively biased positive or negative diode clamper circuit, the failure analysis is also simple and is limited to only a few possible failures.

Initially, the input signal should be checked to determine whether it is present and of correct waveshape and amplitude. If the bias battery or supply voltage should become open no output would be obtained. If the bias supply voltage should become shorted, an output would exist but the reference level would be shifted to zero instead of some positive value. In many cases, a d-c potential exists at the input of the clamper circuit; therefore, it is possible for coupling capacitor C1 to become leaky (or shorted) and cause a voltage divider action to occur. Since capacitor C1 is in series with resistor R1 a continuous current flow can result if the capacitor is leaky (or shorted), and this will produce a change in the reference level at the output of the clamper circuit.

If the value of resistor R1 increases considerably above its original value, distortion of the output waveform is likely to occur, especially when the input waveform is subject to changes in signal amplitude. If the value of R1 decreases considerably, distortion of the output waveform will occur because of the decreased r-c time constant, and as a result, undesirable spikes will be present in the output waveform.

There should be little difficulty in determining the component at fault, since there are only four components in the circuit. Resistor R1 may be measured with an ohmmeter to determine if the value is within tolerance. Capacitor C1 may be checked with a capacitor analyzer or by measuring the voltage from each plate of C1 to ground (if the voltages measured are equal, the capacitor is shorted). If every other component has been checked and the trouble still exists, diode V1 must be at fault.

TRIODE CLAMPER.

A clamping circuit, which is sometimes referred to as a d-c restorer, or a base line stabilizer in other publications holds either extreme of a waveform to a given reference level.

All clamper circuits are dependent on two time constant circuits required to establish the reference level to which the output is clamped, one a long time constant circuit and the other a short time constant circuit. The long time constant circuit is developed by the input coupling capacitor and a resistor, which is shunted by a diode. The short time constant circuit is developed by the input coupling capacitor and the resistance of the diode during the time of its conduction. Whether the clamper is clamped in the positive or negative direction depends upon to which element of the diode the coupling capacitor is connected. If the capacitor is connected to the cathode of the diode the clamping circuit will clamp in a positive direction. If the capacitor is connected to the plate of the diode the clamping circuit will clamp in a negative direction.

Although a diode is sufficient to provide clamping action, is relatively inexpensive, and requires less space and associated circuitry than tubes with more elements, it sometimes become advantageous to use triodes in certain applications. A basic single-tube triode clamper, will provide a higher peak to peak output voltage for a given input voltage

It is necessary that in a basic single-tube triode clamper as in most other triode circuits, that an input coupling capacitor be connected to the grid of the tube in order to prevent d-c coupling. In the case of the basic single-tube triode clamper, the grid of the tube acts as the plate of an effective diode in a diode clamping circuit. Thus with the input coupling capacitor connected to the effective plate of the diode, negative clamping is obtained. However, due to the phase inversion of the input and output signals of an electron tube, positive clamping is obtained at the plate of the triode.

Another type of triode clamper, which uses two tridoes, rather than one is the synchronized triode clamping circuit. This is used in rotating radial sweep radar applications, where a trapezoidal voltage is needed to produce the sweep. The trapezoidal sweep voltage varies above and below a reference line. In addition, the voltage that occurs between sweeps varies in magnitude, from cycle to cycle. As a result, each sweep occurs at a different point on the screen due to the effect of this difference in voltage between sweeps. The synchronized clamper prevents this condition. It is necessarily a two-way clamping circuit because the voltage to be clamped must be clamped both above and below a reference line. The circuit is made inoperative during sweeps, by synchronizing pulses, so that no clamping occurs during the sweep time. Between sweeps, the clamper operates and clamps these undesirable variations in voltage to a reference line from a positive and negative direction. The sychronized triode clamper, and the single triode clamper are discussed separately in the following paragraphs.

BASIC SINGLE-TUBE CLAMPER.

APPLICATION.

A basic single-tube clamper is used where it is desired to obtain amplification of the input signal as well as clamp one extreme of the signal.

CHARACTERISTICS.

Clamping is accomplished between the grid and the cathode, the grid acting as a diode plate.

Clamping between the grid and the cathode can only be in a negative direction, since the coupling capacitor must be connected to the grid of the triode.

Output taken from the plate of the triode will be clamped in a positive direction.

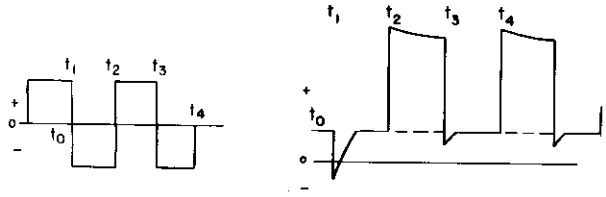
CIRCUIT ANALYSIS.

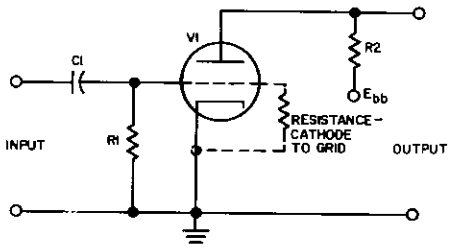
General. The circuit operation of the basic single-tube triode clamper is largely similar to that of the diode clamper. In the triode clamper, the control grid serves the

same function as the diode plate in the diode clamper circuit. The grid-leak bias resistor and coupling capacitor in conjunction with the grid to cathode resistance of the triode provides a means by which two time constants may be produced. These time constants enable a certain bias level to be established, which fixes the reference level to which the output level is clamped.

The grid is maintained at a negative voltage, and since the plate voltage varies inversely and is of opposite polarity, the output voltage is clamped at a positive reference level. The action of the triode also provides amplification of the input signal.

Circuit Operation. A basic single-tube triode clamper is shown in the accompanying illustration. C1 and R1 are the input coupling capacitor and the grid leak bias resistor, respectively. They form the long time constant circuit associated with the clamper. The cathode to grid resistance of triode V1 during the time of maximum conduction along with C1 form the short time constant circuit associated with the clamper. R2 is the plate load resistor, which also provides the proper dc plate voltage to the plate of V1.

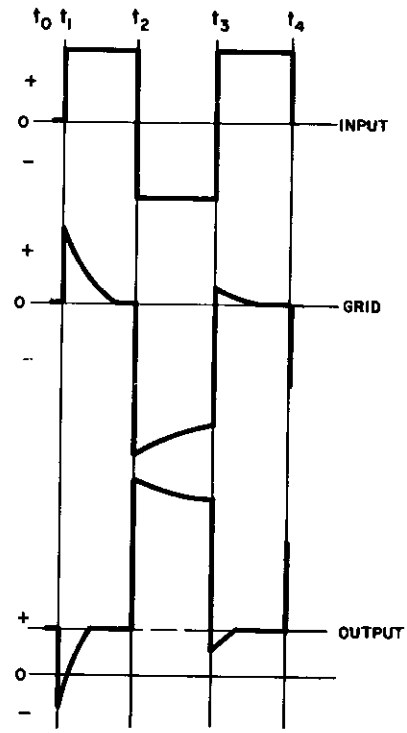




Basic Single-Tube Triode Clamper

The input signal is a typical square wave, having equal positive and negative amplitudes as shown in the accompanying illustration. Prior to the application of the square wave at time t_0, the output voltage is held at a certain level due to the plate voltage being developed across the plate load resistor R2. This voltage value constitutes the reference or clamping level of the output voltage. Times t_1 and t_3 represent the leading edges, and times t_2 and t_4 represent the trailing edges of the input square wave.

At time t_1, the first positive-going leading edge occurs and appears at the grid of V1. Since capacitor C1 cannot



Clamper Waveforms

immediately change its charge the entire voltage appears across R1. Grid current immediately flows from cathode to grid and begins charging capacitor C1. The time required to charge C1 is very short because of the low cathode to grid resistance of V1. As C1 becomes fully charged, the grid side of C1 becomes negative, and the grid is at the same negative potential. This charging action continually reduces the amount of tube conduction from the time of the initial application of the leading edge of the square wave to the time where C1 becomes fully charged. This varies the plate output voltage from some negative value to some positive value (the reference level) where it remains constant for the duration of the pulse, until the trailing edge of the input waveform is reached at time t_2. At t_2, the negative-going trailing edge of the input signal causes a negative voltage to appear across R1 and on the grid of V1. The negative grid swing causes the plate current to reduce, and the plate output voltage, therefore, rises to nearly the full value of the supply (goes positive). At this time, the input signal reaches its maximum negative swing and the output voltage reaches its maximum positive swing. For the duration of the pulse to time t_3 a long time constant path is offered through R1 to discharge C1, since V1 is no longer conducting from grid to cathode (no grid current is flowing). Because

of the long time constant and the relatively short pulse width time, C1 discharges only slightly before the next positive leading edge of the input signal appears at t_3. Thus the output signal drops a few volts. At time t_3 the positive-going input signal drives the grid of V1 positive so that grid current flows. Meanwhile the increased plate current causes the plate voltage to drop below the clamping level because of the slight loss of voltage during the discharge period. Actually, during this period, the grid voltage is driven above zero bias into the positive region and conduction through the short time constant path through the grid to cathode current quickly charges C1 to the clamping level, and removes the overshoot pip on the grid waveform. Thus, the dip in current below the clamping level in the plate circuit is minimized by grid current drawn by V1, and the plate current then remains constant until the trailing edge of the input pulse at t_4. At t_4 the cycle again repeats, and action is the same as described for the period between t_2 and t_4. Actually, the distortion shown in the illustration of the output waveform is exaggerated to facilitate understanding circuit action. In practice the time constant of C1 and R1 is sufficiently large that very little distortion of the waveform occurs.

FAILURE ANALYSIS.

No Output. If a square wave signal within the design limitations of the triode clamping circuit is applied to the input of the circuit a "no output" condition may be the result of no plate voltage existing at the plate of V1. This may be due to a faulty plate supply voltage source or due to an open plate load resistor, R2. The only other faulty component that would result in a "no output" condition is a faulty triode V1.

In order to determine which component is the cause of the "no output" condition, first check to see, with an oscilloscope, if the correct input signal is applied. If a correct signal is applied, check for the presence of plate voltage. If no plate voltage is present, check resistor R2 with an ohmmeter. If R2 is an acceptable value of resistance, check the plate supply voltage source with a high resistance voltmeter to determine if any plate supply voltage exists. If there is no plate supply voltage, try to adjust the source for the correct voltage value. If all these components have been checked and the "no output" condition still exists the triode must be faulty.

Low or Distorted Output. If a "low or distorted output" condition exists it may be due to the square wave input signal not being within the design limitations of the triode clamping circuit. This condition may also be due to any of the following component failures: open or shorted input capacitor C1, open or shorted grid leak resistor R1, shorted plate load resistor R2, incorrect value of plate Ebb, or a defective triode V1.

To determine why the output is low or distorted, first check the square wave input signal with an oscilloscope. Check the capacitor C1 with an in-circuit capacitor checker to determine if it is open, or measure the voltage from both sides of C1 to ground to determine if C1 is shorted. (If the measured voltages are equal the capacitor is shorted.) Check resistor R1 with an ohmmeter. If resistor R1 has an acceptable resistance value, check resistor R2 with an ohmmeter. If resistor R2 has an acceptable resistance value, measure, the value of the plate voltage supply, Ebb, with a high resistance voltmeter. If the plate supply voltage is incorrect, try to adjust the plate voltage supply source for the correct voltage value. If all these components have been checked and the "low or distorted" condition still exists, the triode must be defective.

SYNCHRONIZED TRIODE CLAMPER.

APPLICATION.

A synchronized triode clamper is used in television and radar circuitry where it is desired to hold a signal voltage to a zero reference level and allow the signal to vary both positively and negatively from the zero reference level.

CHARACTERISTICS.

Uses two triodes connected in series.
Clamping occurs between input signal variations.
Synchronizing pulses are required.

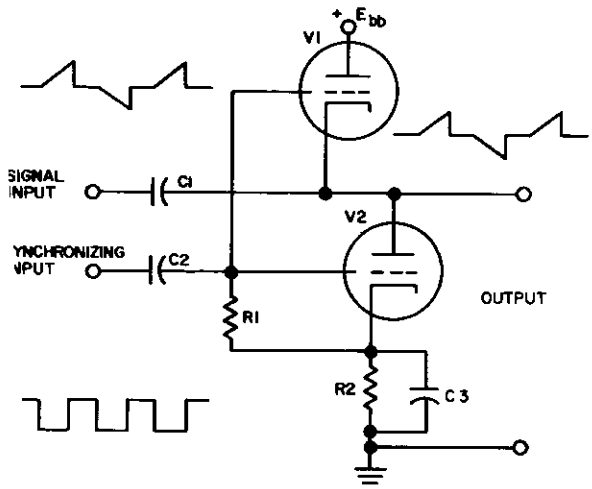
CIRCUIT ANALYSIS.

General. A synchronized triode clamper utilizes the conduction of two triodes to maintain a specific reference level during the time that no signal is present. At the time that the input signal occurs, a negative synchronizing pulse drives the triodes into a nonconducting state for the duration of the synchronizing pulse. The duration of the synchronizing pulse and the duration of the input signal are the same. Any variation in the voltage between input signals (when the triodes are conducting) changes the amount of conduction of the triodes and changes the amount of plate voltage and plate resistance of the triodes. The change in plate voltage and plate resistance is such that the output voltage is maintained at the reference level.

Circuit Operation. A typical triode clamping circuit is shown in the accompanying illustration. The input is coupled through capacitor C1 directly to the output. The series combination of triode V1, triode V2, and cathode bias resistor R2 intersects this input line (between capacitor C1 and the output) at the point where the cathode of V1 and the plate of V2 are connected. Capacitor C2 couples a series of negative synchronizing pulses to the grids of triodes V1 and V2. Resistor R1 develops a potential difference (bias) between the cathode and the grid of V2 during the time of the synchronizing pulse. Capacitor C3 is an a-c bypass capacitor for cathode bias resistor R2.

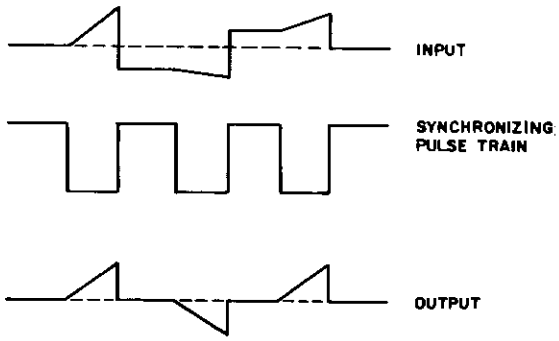
The input signal, in this case, is a series of positive and negative going sawtooth waveforms extending from the zero voltage reference line. There is a steady-state period with no signal variation between the sawtooth waveforms.

A synchronizing pulse signal is applied to capacitor C2. This synchronizing pulse signal consists of negative pulses equal in duration to and occurring at the same time



Synchronized Triode Clamper

as the sawtooth waveforms. The period between each sawtooth, therefore, is equal to the period between each synchronizing pulse. A diagram of the corresponding time and amplitude relationships of the input, synchronizing, and output waveforms is shown in the accompanying illustration.



Clamper Waveforms

At the time either a positive or negative sawtooth waveform is applied to the input of capacitor C1, a negative synchronizing pulse is applied to the synchronizing input through capacitor C2 and applied to the grids of triodes V1 and V2. This synchronizing pulse cuts off the triodes V1 and V2 for the duration of the pulse, which is equal to the period of the sawtooth waveform. When the duration of the sawtooth waveform ends, the duration of the synchronizing pulse is likewise completed, and triodes V1 and V2 return to conduction, forming a voltage divider network. This voltage divider consists of the two triodes and a cathode bias resistor R2 in a series connection, extending between plate voltage supply Ebb and ground.

If there should be any voltage at the input that varies from the zero reference line, at this time, the conduction of the triodes will vary in such a way as to compensate for the voltage variation and to maintain the output at the zero reference. If this voltage variation is positive, the voltage at the cathode of V1 and the voltage at the plate of V2 is made more positive. The increased plate voltage of V2, in most cases, is relatively ineffective in changing the amount of conduction of V2. The increased voltage at the cathode of V1, however, causes the grid voltage to appear more negative, thereby increasing the bias. (This positive increase in voltage is then much more effective in changing the conduction of V1 than in changing the conduction of V2). The conduction of V1 is then reduced causing the plate resistance of V1 to increase, thereby causing a greater voltage drop across V1. With the increased voltage drop across V1, there will be less voltage available at the plate of V2, and thus at the output. This voltage decrease at the plate of V2 and at the output is equal to the positive voltage variation occurring at the input. The output voltage is, therefore, maintained at the zero reference level.

If the voltage variation, at the time that triodes V1 and V2 are in the state of conduction, is negative, the voltage at the plate of V2 and at the cathode of V1 is negative. The voltage decrease at the cathode of V1 causes the grid voltage to appear more positive, thereby decreasing the bias. (This decrease in voltage is then much more effective in changing the conduction of V1 than in changing the conduction of V2.) The conduction of V1 is increased causing the plate resistance of V1 to decrease and causing the voltage drop across V1 to decrease. A more positive voltage is then present at the cathode of V1, at the plate of V2 and at the output. This voltage increase is equal to the negative voltage variation at the input. Thus output voltage is maintained at the zero reference level for a negative voltage variation as well as a positive voltage variation.

FAILURE ANALYSIS.

No Output. A "no output" condition may be due to any of the following failures: an open coupling capacitor C1, an open synchronizing pulse capacitor C2, no input signal, or no synchronizing pulse train. These failures may be located by measuring capacitors C1 and C2 with an in-circuit capacitor checker, and by observing the input signal with an oscilloscope. If either the input signal or the synchronizing pulse train is not present at the respective inputs, check the input signal source or the synchronizing pulse source with an oscilloscope. If the "no-output" condition still exists after these checks have been made, a bad connection somewhere in the circuit must be the cause.

Low or Distorted Output. A low or distorted output may be due to any of the following defects (provided the proper input signal is applied): low or no plate supply voltage, improper synchronizing pulse, open or shorted resistor R2,

open or shorted resistor R1, open or shorted capacitor C3, shorted capacitor C1, shorted capacitor C2, or, if the condition still exists after checking these components, triode V1, or triode V2, or both triodes must be defective.

To determine which of these components is at fault, first check the input signal with an oscilloscope. If the input signal is correct, proceed to the synchronizing pulse input and check the synchronizing pulse train with an oscilloscope. If either the input signal or the synchronizing signal is incorrect the trouble is not in the clamping circuit, but is in some stage prior to the clamper. If the synchronizing pulse train is correct, check the plate supply voltage with a high resistance voltmeter. If the plate supply voltage is correct, check resistors R1 and R2 with an ohmmeter. Check capacitor C3 with an in-circuit capacitor checker, or by measuring the voltage from both plates of C3 to ground. If both voltages are equal the capacitor is shorted. If all components are found to be satisfactory the fault must be in either triode V1 or triode V2, or in both triodes.

At time t_4 the input signal again drops from +10 to +2 volts. The 8 volt drop appears as a negative output across R1 causing the output voltage to drop from zero to -8 volts. Once again, C1 begins to discharge through the long time constant circuit as explained previously.

The output waveform has been purposely drawn to show a substantial decrease in voltage caused by the discharge of C1 during the duration of the negative peak of the input waveform (times t_2 to t_3 and t_4 to t_5). In practice, however, the value of R1 is relatively large so that little distortion results from the discharging of C1 or from its charging through CR1. The semiconductor diode, however, does have a much lower reverse resistance that of the electron tube. Since this back resistance is effectively connected in parallel with R1, it lowers the overall output resistance and reduces the value of the long time constant. Therefore, more distortion is produced by the semiconductor diode clamper than the tube diode.

From the explanation of circuit operation given above, it is seen that the positive extreme of the input waveform has been held or clamped to zero reference level, and that the entire waveform has been shifted negatively with respect to this reference level.

FAILURE ANALYSIS.

General. Because of the extreme simplicity of the negative diode clamper circuit, there are only a few possibilities of trouble. The capacitor, resistor, and diode can be checked for shorted or open-circuited conditions with an ohmmeter. Circuit functioning, however, must be checked with an oscilloscope to determine whether the waveform is correct and the operation is normal.

No Output. An open-circuited capacitor, a lack of input signal, or a shorted or defective diode can cause a no-output indication. Use an oscilloscope to determine whether the proper input signal is present and whether it appears across R1.

Low Output. A leaky or partially shorted capacitor can cause other than normal output. Usually such a condition will be indicated by a change in the d-c voltage measured across R1, assuming a normal input signal. A defective diode can also cause this condition, and is usually indicated by a much-lower-than-normal reverse resistance.

Distortion. Normally there should be no distortion of the output signal. Any distortion visible on an oscilloscope (with a frequency response high enough for the pulse used) indicates a change in circuit time constants due to defective components. Use an "in-circuit" type of capacitor checker to determine whether the capacitor is leaky. The remaining elements can be checked with an ohmmeter. (Be certain to observe the proper polarity when checking the diode; otherwise, an erroneous indication will be obtained.)

Clamping Level Changes. A change in the clamping level could be caused by a defective diode, a leaky coupling capacitor, C1, or a change of input pulse amplitude. As long as the input pulse amplitude is constant clamping will occur as described above. If, however, the pulse amplitude varies from pulse to pulse, the low amplitude pulses will not be properly restored. This action occurs because the low amplitude pulse is unable to reach the zero level or rise above it. Thus the diode can not operate to restore the charge lost in the discharging of capacitor C1 through the long time constant circuit between pulses. Hence the following pulse will start at some point below the zero level. If excessive, it may be possible to read a negative voltage across R1.

In the case of a leaky capacitor, the diode will conduct constantly for a positive voltage (NPN collector polarity) applied to the anode, or with a constant negative voltage (PNP collector polarity) applied it will act as a biased type clamp. This condition may be determined by making a voltage check with a VTVM connected across the output of the clamp.

POSITIVE-DIODE CLAMPER.

APPLICATION.

The positive diode clamper (or DC restorer) is used where it is desired to hold, or "clamp", the negative extreme of a waveform to a zero reference level (the reference level for this circuit must be ground potential). This circuit is commonly used in radar, television, telemetering, and computers.

CHARACTERISTICS.

Input signal contains both positive and negative portion, but output signal consists only of a positive-going signal similar to the input signal.

Input and output signals are in phase with each other.

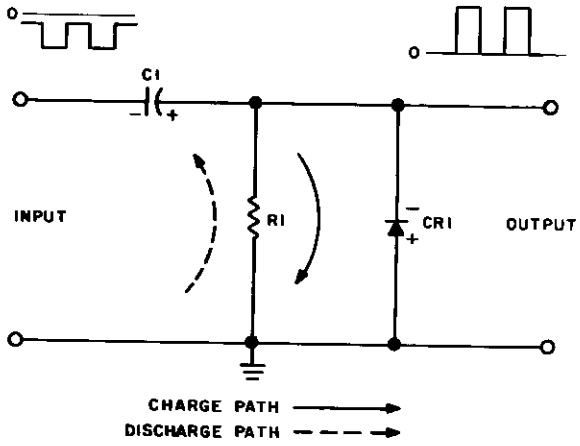
Used in conjunction with an RC coupling network.

CIRCUIT ANALYSIS.

General. The unbiased diode clamp is usually employed as a shunt across the resistor portion of an RC coupling circuit. By providing a low resistance path during conduction periods and a high resistance path during nonconducting periods, the diode provides different charge and discharge times for the coupling capacitor. When the negative portion of the input waveform causes the diode to conduct, positive clamping is produced, as described in the following paragraph.

Circuit Operation. The schematic of a basic unbiased diode clamp is shown in the accompanying illustration. As shown, C1 is the coupling capacitor of an RC coupling network. Resistor R1 is the input resistor of the network and determines the long time constant (discharge period) of the circuit. Clamping diode CR1 connected in shunt with R1 determines the short time constant (charging time) of the circuit. When a negative input signal is applied it causes CR1 to conduct, and C1 is quickly charged to the input potential. Since the output is taken from across R1, which is effectively short circuited by the conducting diode (forward resistance is only a few ohms), little or no output appears for the negative portion of any applied signal. During the positive portion of the input signal CR1 does not conduct (except for reverse leakage current) consequently

the positive portion of the input signal appears as the output across R1. This circuit acts to effectively shift the entire waveform in a positive direction by holding the negative peak of the input signal to the zero level. Therefore, the input waveform can only appear as a positive output. Thus the negative portion is effectively eliminated by the clamping diode.

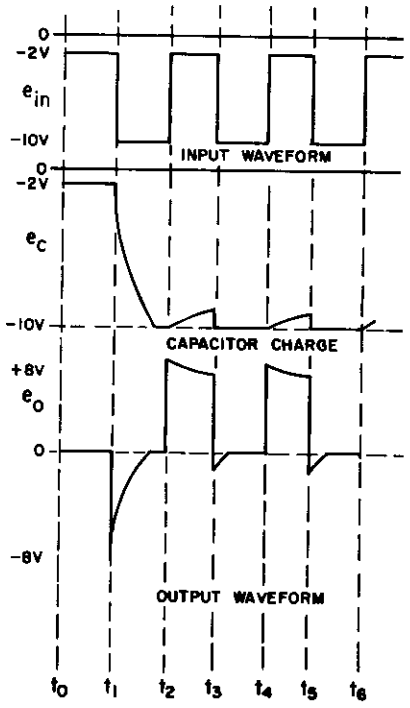


Positive Clamper

In the following waveform illustration the input waveform is shown as a square wave for ease of explanation. Likewise, the input waveform level is considered to vary from -2 to -10 volts. Such an input waveform is typical of the waveform generated at the collector of a PNP transistor multivibrator. Although a square wave is used in the following explanation of detailed circuit operation, any waveshape applied to the clamper input will be positively clamped without appreciably changing the shape of the wave (provided that the R1-C1 time constant is long with respect to the pulse duration).

Capacitor C1 is charged as indicated in the waveform illustration to a potential of -2 volts at the positive peak of the input waveform (t_0). At time t_1 the input to the clamper circuit drops 8 volts to a -10 volts. Since capacitor C1 cannot change its charge immediately the 8 volt change appears across R1 and CR1 producing a negative spike on the output waveform. Since the anode of CR1 is now effectively 8 volts positive with respect to its negative cathode, CR1 conducts and charges C1 to -10 volts. The charging of C1 occurs rapidly because of the low forward resistance of the diode, and the low forward resistance of the diode shunting R1 causes any output voltage to drop to zero during time t_1 to t_2. Simultaneously, the diode stops conducting, and capacitor C1 remains in its charged condition for the duration of the pulse.

At t_2 the input signal rises 8 volts (from -10 volts to -2 volts). Since C1 is charged to -10 volts and cannot discharge immediately through the long time constant circuit created by R1, this positive-going voltage appears across R1 as a positive 8 volt output. (CR1 cannot conduct because its cathode is now positive with respect to its anode.) Thus at point t_2 on the waveform, the input voltage rises from -10 volts to -2 volts and the output rises from zero to +8 volts. Between pulses, during the time interval from t_2 to t_3, capacitor C1 discharges slightly (say from -10 volts to -9 volts) through the long time constant path of R1.



Clamper Input and Output Waveforms

At point t_3 of the input waveform the input signal again falls 8 volts (from -2 volts to -10 volts). Once again the charge on C1 cannot change immediately and the 8 volt negative change appears across R1. Because of the previously assumed discharge of 1-volt through R1 between time t_2 and t_3, the 8 volt change now exceeds the capacitor charge voltage. Therefore, the output voltage overshoots the zero reference level, and a negative (approximately 1-volt) signal appears across R1 and CR1. With the cathode of CR1 negative with respect to its anode, the diode conducts momentarily and replaces the slight loss of charge on C1. As a result, the output voltage quickly drops to zero and remains at zero level until the end of the pulse at time t_4.

At time t_4, the input signal again increases from -10 to -2 volts. The 8 volts increase appears as a positive output across R1 causing the output voltage to rise from zero to +8

volts. Once again C1 begins to discharge through the long time constant circuit as explained previously.

The output waveform has been purposely drawn to show a substantial decrease in voltage caused by the discharge of C1 during the duration of the positive peak of the waveform (times t_2 to t_3 and t_4 to t_5). In practice, however, the value of R1 is relatively large so that little distortion results from the discharging of C1 or from its charging through CR1. The semiconductor diode, however, does have a much lower reverse resistance than that of an electron tube. Since this back resistance is effectively connected in parallel with R1, it lowers the overall output resistance and reduces the value of the long time constant. Therefore, more distortion is produced by the semiconductor diode clamper than the tube diode.

From the explanation of circuit operation given above, it is seen that the negative extreme of the input waveform has been held or clamped to the zero reference level, and that the entire waveform has been shifted positively with respect to this reference level.

FAILURE ANALYSIS.

General. Because of the extreme simplicity of the negative diode clamper circuit, there are only a few possibilities of trouble. The capacitor, resistor, and diode can be checked for shorted or open-circuited conditions with an ohmmeter. Circuit functioning, however, must be checked with an oscilloscope to determine whether the waveform is correct and the operation is normal.

No Output. An open circuited capacitor C1, a lack of input signal, or a shorted or defective diode can cause a no-output condition. Use an oscilloscope to determine whether the proper input signal is present and whether it appears across R1.

Low Output. A leaky or partially shorted capacitor, C1, can cause other than normal output. Usually such a condition will be indicated by a change in the dc voltage measured across R1, assuming a normal input signal. A defective diode can also cause this condition, and is usually indicated by a much-lower-than-normal reverse resistance.

Distortion. Normally, there should be no distortion of the output signal. Any distortion visible on an oscilloscope (with a frequency response high enough for the pulse used) indicates a change in circuit time constants due to defective components. Use an "in-circuit" type of capacitance checker to determine whether the capacitor is leaky. The remaining elements can be checked with an ohmmeter. (Be certain to observe the proper polarity when checking the diode; otherwise, an erroneous indication will be obtained.)

Clamping level Changes. A change in the clamping level could be caused by a defective diode, a leaky coupling capacitor, C1, or a change of input pulse amplitude. As long as the input pulse amplitude is constant clamping will occur as described above. If, however, the pulse amplitude varies from pulse to pulse, the low amplitude pulses will not be properly restored. This action occurs because the low amplitude pulse is unable to reach the zero level or drop below it. Thus the diode cannot operate to restore the charge lost in the discharging of capacitor C1 through the long time constant circuit between pulses. Hence the following pulse will start at some point above the zero level. If excessive, it may be possible to read a constant positive voltage across R1.

In the case of a leaky capacitor, the diode will conduct constantly for a negative voltage (PNP collector polarity) applied to the cathode, or for the opposite case (NPN transistor) it will act as a biased type of clamp. This condition may be checked by making a voltage check with a VTVM connected across the output of the clamp.

BIASED-NEGATIVE DIODE CLAMPER

APPLICATION.

The biased-negative diode clamper is used in transistorized equipment when it is desired to shift the reference level of the applied signal in a negative direction. This type of circuit is commonly used in radar, television, and computers.

CHARACTERISTICS.

Establishes the d-c reference level of the waveform, but does not affect its amplitude.

Uses a diode in conjunction with an R-C coupling circuit.

Can clamp either extreme of the input waveform to the negative reference level, by reversing the diode.

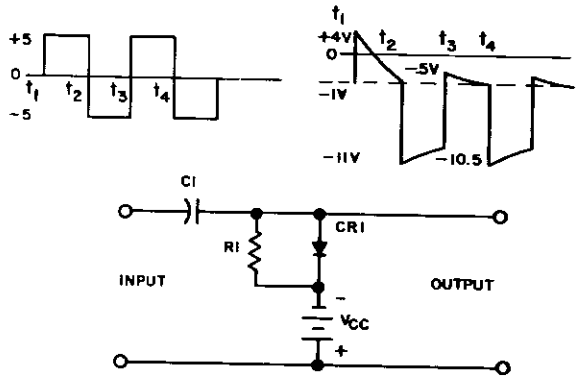
Reference level established by the amount of negative bias used.

CIRCUIT ANALYSIS.

General. The biased negative diode clamper may be of either the positive or negative type, depending upon the relative connection of the diode with respect to the bias. Under all circumstances, the reference level of the negatively-biased diode clamper will be at some negative value. If it is a negatively-biased positive diode clamper, the output waveform will start at this negative value and extend in a positive direction. If it is a negatively-biased negative diode clamper, the output waveform will start at this negative reference level, and extend in a negative direction. The circuit is comprised basically of a diode and an RC network. The diode acts as a switch, closing on one half cycle to provide a very short RC time for the capacitor, and opening on the alternate half cycle, to provide a long time constant which depends upon the size of a resistor in conjunction with the capacitor. The overall result at the output is a reproduction of the input, but shifted to a new reference level.

Circuit Operation. A typical negatively-biased negative diode clamper is illustrated below.

Capacitor C1 and resistor R1 form an RC coupling network and determine the long time constant associated with the circuit. Diode CR1, during the time of its conduction, together with C1, determine the short time constant associated with the circuit. The bias supply, V_{CC}, alters the reference level from zero to a level equal to the bias.



Negatively-Biased Negative Diode Clamper

When the circuit is initially energized and with no signal applied to the input, the diode begins conducting because of the negative potential (V_{CC}) applied to the cathode. As CR1 conducts, capacitor C1 begins charging, and when its charge is equal to V_{CC}, the diode cuts off, since its anode and cathode potentials are now equal. The voltage at the output is at this time equal to the bias voltage V_{CC}, or −1 volt.

When a signal is applied, as illustrated, the following action occurs. At time t_1, the voltage increases almost instantly from 0 volts to a +5 volts. (The voltages used here are only for ease of explanation). Capacitor C1 cannot change its charge immediately (because of the property of capacitors), and the anode of CR1 suddenly becomes more positive than its cathode and begins conducting. Because C1 cannot immediately change its charge, the entire input voltage is developed across the diode, and the output, taken from across the diode, increases 5 volts in a positive direction. Because it does not start at 0 volts, but at 0 −1 volt, as shown on the illustration, the output rises to +4 volts. The conducting state of CR1 provides a very short time constant for the capacitor, however, and C1 rapidly charges to the new voltage. As C1 charges, the voltage drop across CR1 decreases, and once again reaches −1 volt when C1 is fully charged.

The output remains at this voltage until the negative swing of the input signal at time t_2. At this time the input swings from a +5 volts to a −5 volts. Again, C1 cannot immediately change its charge, but this time the diode cannot conduct, because its anode is negative with respect to its cathode. The entire input voltage is therefore developed across R1, and the output voltage changes 10 volts in a negative direction from the −1-volt reference level, or to −11 volts. Because the diode is not conducting, R1 provides a long time constant for C1 and the capacitor begins charging very slowly to the −5 volts of the input signal. The capacitor charges very slowly because of the long RC time constant, and when the input signal reaches t_3, the total output has only decreased to, for example, from −11 to −10.5 volts (the capacitor has charged to .5 volt). At time t_3, the input again rises to +5 volts, bringing CR1 into conduction. This sudden +10 volt rise also produces a +10 volt increase in the output. Since the total output is 10.5 volts at this time, a +10 volt increase brings it up to −.5 volts, which accounts for the small positive-going peak at t_3 in the output waveform. Because of the short RC time provided by CR1, the capacitor quickly charges again to −1 volt eliminating the peak, and the output remains a −1 volt until time t_4, when the cycle again repeats.

By reversing the diode, the circuit can be converted into a negatively-biased, positive diode clamper. The difference at the output then will be that the entire output waveform will be clamped above the negative bias voltage, instead of below it as in the negative clamper.

Because the reverse resistance of a semiconductor diode is lower than that of an electron tube, the type of diode used is selected to have a very high reverse resistance. This is necessary to keep the shunting effect of the reverse resistance to a minimum.

FAILURE ANALYSIS.

No Output. The absence of an input signal, or an open C1 are the only probable causes of a no-output condition. Check for the presence of the input signal with an oscilloscope. If signal is not present, the fault lies in a preceding stage, and the clamper is probably not defective. If a signal is present, check C1 with an in-circuit capacitor checker. There is also the possibility that two components such as CR1 and V_{CC}, or R1 and V_{CC}, are both shorted at the same time, thus producing a short circuit across the output. Check the bias supply with a high resistance voltmeter for proper voltage, and R1 and CR1 with an ohmmeter. Care should be used in checking the diode, as erroneous indications may be obtained by not observing proper polarities. For the special case where the diode is not completely shorted, but reads a very low resistance of, say 2000-ohms or less, it can be considered to be defective.

Low or Distorted Output. A partially shorted CR1, a leaky C1, or R1 decreasing in value can cause a low output condition to exist. Actually, the output will not be low without being distorted, nor will it be distorted without being low. Check C1 with an in-circuit capacitor checker, and R1 and CR1 with an ohmmeter. Care should be used in checking the diode, as erroneous indications may be obtained by not observing proper polarities. For the case where the diode is not completely shorted, but reads a very low resistance of, say 2000-ohms or less, it can be considered to be defective.

Change in Clamping Level. A change in the bias supply voltage, V_{CC}, will cause the output clamping level to change. Check for the proper value of voltage with a high resistance voltmeter.

BIASED-POSITIVE DIODE CLAMPER.

APPLICATION.

The biased-positive diode clamper is used in transistorized equipment when it is desired to shift the reference level of the applied signal in a negative direction. This type of circuit is commonly used in radar, television, and computers.

CHARACTERISTICS.

Establishes the d-c reference level of the waveform but does affect its amplitude.

Uses a diode in conjunction with an R-C coupling circuit.

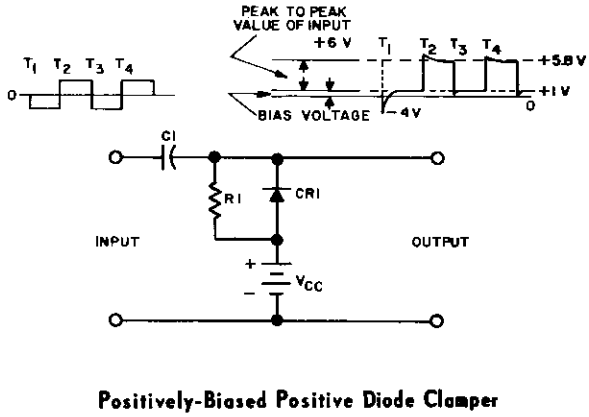
Can clamp either extreme of the input waveform to the positive reference level, by reversing the diode.

Reference level established by the amount of positive bias used.

CIRCUIT ANALYSIS.

General. The biased positive diode clamper may be of either the positive or negative type, depending upon the relative connection of the diode with respect to the bias. Under all circumstances, the reference level of the positively-biased diode clamper will be at some positive value. If it is a positively-biased positive diode clamper, the output waveform will start at this positive value and extend in a positive direction. If it is a positively-biased negative diode clamper, the output waveform will start at this positive reference level, and extend in a negative direction. The circuit is comprised basically of a diode and an RC network. The diode acts as a switch, closing on one half cycle to provide a very short RC time for the capacitor, and opening on the alternate half cycles, to provide a long time constant which depends upon the size of a resistor in conjunction with the capacitor. The overall result at the output is a reproduction of the input, but shifted to a new reference level.

Circuit Operation. A typical positively-biased positive diode clamper is illustrated below.



Positively-Biased Positive Diode Clamper

Capacitor C1 and resistor R1 form an RC coupling network and determine the long time constant associated with the circuit. Diode CR1, during the time of its conduction, together with C1, determine the short time constant associated with the circuit. The bias supply, Vcc, alters the reference level from zero to a level equal to the bias.

When the circuit is initially energized and with no signal applied to the input, the diode begins conducting because of the positive potential (Vcc) applied to the anode. As CR1 conducts, capacitor C1 begins charging, and when its charge is equal to Vcc, the diode cuts off, since its anode and cathode potentials are now equal. The voltage at the output is at this time equal to the bias voltage Vcc, or +1 volt.

When a signal is applied, as illustrated, the following action occurs. At time t_1, the input voltage increases almost instantly from 0 volts to a -5 volts. (The voltages used here are only for ease of explanation). Capacitor C1 cannot change its charge immediately (because of the property of capacitors), and the anode of CR1 suddenly becomes more positive than its cathode and begins conducting. Because C1 cannot immediately change its charge, the entire input voltage is developed across the diode, and the output, taken from across the diode, increases 5 volts in a negative direction. Because it does not start at 0 volts, but at the bias level of +1 volt, as shown on the illustration, the output decreases to only a negative 4 volts. The conducting state of CR1 provides a very short time constant for the capacitor, however, and C1 rapidly charges to the new voltage. As C1 charges, the voltage drop across CR1 decreases, and once again reaches +1 volt when C1 is fully charged.

The output remains at this voltage until the positive swing of the input signal at time t_2. At this time the input swings from a -5 volts to a +5 volts. Again, C1 cannot immediately change its charge, but this time the diode cannot conduct, because its anode is negative with respect to its cathode. The entire input voltage is, therefore, developed across R1, and the output voltage changes 5 volts in a positive direction from the +1 volt reference level, or to +6 volts. Because the diode is not conducting, R1 provides a long time constant for C1 and the capacitor begins charging very slowly to the +5 volts of the input signal. The capacitor charges very slowly because of the long RC time constant, and when the input signal reaches t_3, the total output has only decreased, for example, from +6 volts to +5.8 volts (the capacitor has charged to .2 volt). At time t_3, the input again changes to -5 volts, bringing CR1 into conduction. This sudden change to -5 volts also produces -5 volts at the output. Since the total output is +5.8 volts at this time, a -5 volt change brings it down to +.8 volt, which accounts for the small negative going peak at t_3 in the output waveform. Because of the short RC time provided by CR1, the capacitor quickly charges again to +1 volt, eliminating the peak and the output remains at +1 volt until time t_4, when the cycle again repeats.

By reversing the diode, the circuit can be converted into a positively biased, negative diode clamper. The difference at the output then will be that the entire output waveform will be clamped above the positive bias voltage, instead of below it as in the negative clamper.

Because the reverse resistance of a semiconductor diode is lower than that of an electron tube, the type of diode used is selected to have a very high reverse resistance. This is necessary to keep the shunting effect of the reverse resistance to a minimum.

FAILURE ANALYSIS.

No Output. The absence of an input signal, or an open C1 are the only probable causes of a no-output condition. Check for the presence of the input signal with an oscilloscope. If the signal is not present, the fault lies in a preceding stage, and the clamper is probably not defective. If a signal is present, check C1 with an in-circuit capacitor checker. There is also the possibility that two components such as CR1 and V_{CC}, or R1 and V_{CC}, are both shorted at the same time, thus producing a short circuit across the output. Check the bias supply with a high resistance voltmeter for proper voltage, and R1 and CR1 with an ohmmeter. Care should be used in checking the diode, as erroneous indications may be obtained by not observing proper polarities. For the special case where the diode is not completely shorted, but reads a very low resistance, of say 2000 ohms or less, it can be considered defective.

Low or Distorted Output. A partially shorted CR1, a leaky C1, or R1 decreasing in value can cause a low output condition to exist. Actually, the output will not be low without being distorted nor will it be distorted without being low. Check C1 with an in-circuit capacitor checker, and R1 and CR1 with an ohmmeter. Care should be used in checking the diode, as erroneous indications may be obtained by not observing proper polarities. For the case where the diode is not completely shorted, but reads a very low resistance of, say 2000 ohms or less, it can be considered defective.

Change in Clamping Level. A change in the bias supply voltage, V_{CC}, will cause the output clamping level to change. Check for the proper value of voltage with a high resistance voltmeter.

TRIODE, BASIC COMMON-BASE CLAMPER.

APPLICATION.

The basic common-base triode clamper maintains between specific voltage levels the maximum positive and negative voltages developed at the collector of the transistor used in the clamping circuit. This circuit is usually used as a switching amplifier to maintain a constant output pulse amplitude.

CHARACTERISTICS.

Common base transistor configuration provides an output with no current amplification and no phase inversion.

Collector voltage is clamped, not the output voltage.

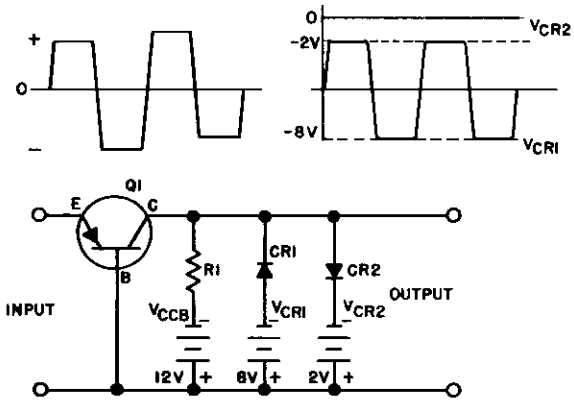
Two diodes provides clamping action.

Diode bias potentials establish minimum and maximum clamping levels.

CIRCUIT ANALYSIS.

General. The clamping action to be discussed occurs in the collector circuit of the common base connected transistor. Normally, the signal voltage in conjunction with the series combination of the collector load resistor and the collector supply voltage develops a certain collector voltage. If the input signal varies above some level, however, one of two diodes begins conducting. These diodes are connected in parallel with each other and with the collector supply and load. The conduction of the diode maintains or clamps the collector voltage at the bias value. If the signal varies below some level in the opposite direction the other diode conducts, causing the collector voltage to be maintained or clamped at another lower voltage level. During the time that the signal is between clamping levels, the collector voltage varies in accordance with the input signal voltage variation.

Circuit Operation. The circuit of the triode, basic common-base clamper used in this application is shown in the accompanying illustration.



Triode, Basic Common Base Clamper

The input signal voltage, as illustrated, is a square-wave pulse type signal which may vary from maximum to minimum amplitudes. It is applied to the emitter of transistor Q1, connected in a common base configuration. The collector voltage variation corresponds to the input voltage variation and is developed across the collector load resistor, R1, by the collector supply voltage V_{CCB}. Diode CR1 and its base voltage V_{CR_1}, establish a negative clamping level, below which the collector voltage cannot go. Diode CR2 and the bias voltage V_{CR_2}, establish a positive clamping level above which the collector voltage cannot go.

The input signal applied to the emitter of Q1 is amplified and in-phase when it appears as the output voltage at the collector of Q1. If the output voltage developed at the collector of Q1 is between the voltage limits of V_{CR_1} and V_{CR_2} the diodes cannot conduct. The collector voltage varies in accordance with V_{CCB} minus the output voltage developed across R1 (V_{R_1}), which depends upon the collector current. Once the input signal varies enough to cause the positive collector voltage swing to exceed the value of V_{CR_2} (assumed to be −2 volts), diode CR2 conducts because the anode is driven positive and forward-biases the diode. The collector voltage is then maintained at the value of V_{CR_2} until the signal voltage drops to a point at which the positive collector voltage swing becomes less than the voltage V_{CR_2}, at which time CR2 becomes reverse biased, stops conducting, and the collector voltage is again dependent on V_{CCB} minus V_{R_1}.

If the input signal varies enough in the opposite (negative) direction to cause the collector voltage to become the same as, or more negative than the value V_{CR_1} (assumed to be −8 volts) diode CR1 is forward-biased and conducts. The collector voltage is then maintained at the value of V_{CR_1} until the signal voltage increases to a value where the collector voltage becomes more positive than the voltage V_{CR_1}, at which time diode CR1 is reverse biased, stops conducting, and the collector voltage is again dependent on V_{CCB} minus V_{R_1}.

By clamping both the positive and negative levels, the transistor is prevented from saturating and causing hole storage effects which would increase the pulse length, or from being driven to cutoff when the input is in the other direction. It also has the advantage of not requiring special selection of transistors at the time of replacement, since the operating limits are made such that any transistor of the same type will operate satisfactorily in this circuit. This circuit is not used with sine-wave inputs except where clipping effects are desired.

FAILURE ANALYSIS.

No-Output. A no-output condition may prevail due to any of the following defects: no input signal present at the emitter of Q1, an open or shorted collector supply voltage V_{CCB}, an open collector load resistor, R1, or a defective transistor, Q1.

The location of the cause of the no-output condition may be found by first determining if an input signal is present with an oscilloscope. If the input signal is present, check collector supply voltage, V_{CCB}, with a voltmeter. If the collector supply voltage is present check resistor R1 with an ohmmeter. If all other possibilities have been checked and a no-output condition still exists, transistor Q1 can be considered defective.

Low or Distorted Output. This condition may be due to a faulty input signal. If the input signal is found to be correct by an oscilloscope the low or distorted output condition may be due to any of the following conditions: improper voltage values for, collector supply voltage V_{CCB}, bias voltage V_{CR_1}, or bias voltage V_{CR_2}; shorted or open diodes CR1 or CR2; or a load resistance (R1) which is not the proper resistance value; or a defective transistor, Q1.

To determine which of the possible causes of the low or distorted output condition is responsible; first, check the voltage values V_{CCB}, V_{CR_1}, and V_{CR_2} with a high resistance voltmeter. If any of these values is incorrect adjust the particular voltage source for the proper value. If these voltages are correct, check diodes CR1 and CR2 with an ohmmeter. If the diodes are good, the ohmmeter will read zero resistance when placed across the diode in a forward direction, and will read infinite resistance or a very high resistance when placed across the diode in the reverse direction. If the diodes are good, check resistor R1 with an ohmmeter. If all of the preceding items have been checked and found satisfactory, transistor Q1 must be the faulty component.

R-L DIFFERENTIATOR.

APPLICATION.

The R-L differentiator is used to distort an applied waveform (such as a square wave) into a peaked wave for the purpose of providing trigger and marker pulses. It is also used to electronically perform the mathematical function of differentiation in computers, and for separating the horizontal sync in television receivers.

CHARACTERISTICS.

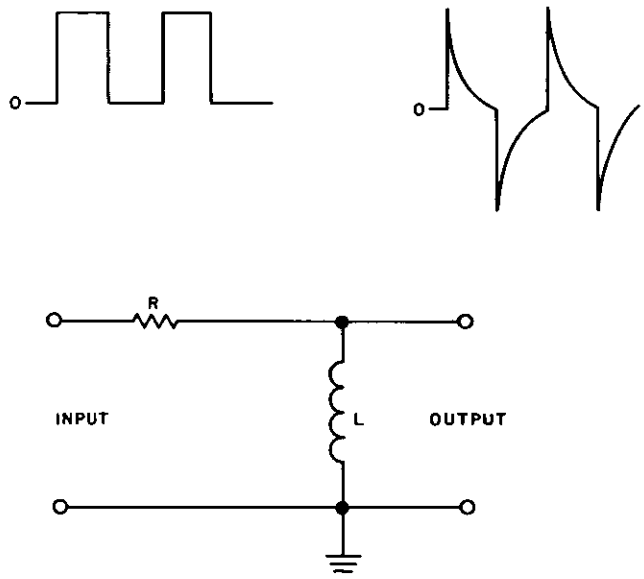
Produces distortion of the input waveform.
Has a short time constant.
Output is taken from across inductor.
Functions essentially as a high-pass filter.
Output is similar to the output of an R-C differentiator.

CIRCUIT ANALYSIS.

General. The output of a differentiator is proportional to the rate of change of the input signal. For a rising (positive going) input the differentiator produces a positive pulse, for a falling (negative going) input it produces a negative pulse, and for a constant input it produces no output. The differentiator electronically simulates the matehmatical operation of taking the first derivative. Second, third, and fourth derivatives may be obtained by cascading an equivalent number of differentiators. Theoretically the differentiator is accurate only when the output voltage is very small in comparison with the input voltage. In practice, this is achieved by using the shortest possible time constant for the highest frequency component involved in the waveform being differentiated. For computer, fire control, and similar operations, differentiation of the basic signal voltage produces an output voltage that represents the speed of the object, double differentiation yields the rate of change of acceleration. For timing and synchronizing use, a sharp pulse is produced for each leading edge and trailing edge of the input waveform.

Circuit Operation. A schematic of a basic R-L differentiator is shown in the accompaning illustration.

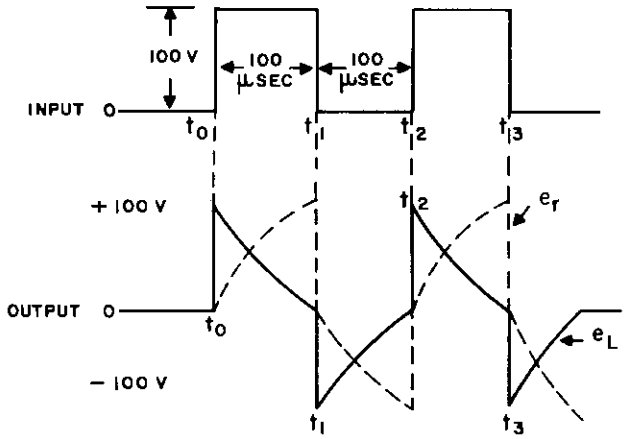
The input is applied between the resistor and ground, and the output is taken across the inductor. The time constant (in seconds) of an R-L circuit is found by dividing the inductance (in Henrys) by the resistance (in ohms) TC=L/R. Thus to shorten the time constant of an L-R circuit it is necessary to increase resistance R rather than decrease R as in the R-C circuit. The counter emf produced in an inductor causes it to have the property of opposing any change in current flow. By referring to the universal time-constant chart in Section 2 of the Handbook, it is noted that the inductor voltage decreases from the applied voltage at an exponential rate to approximately zero at the end of 5L/R time intervals. Likewise, when the source is removed, a counter emf of opposite polarity is induced in the inductor, and this tends to keep current flowing. This voltage also decreases at an exponential rate. Thus, if a square pulse having a time duration of 5L/R time intervals is applied, a



Basic R-L Differentiator Circuit

peaked waveform appears as the output voltage. This output waveform has a shape that is similar to the output obtained from an R/C differentiator.

The exact functioning of the differentiator may be easier understood by referring to the accompanying illustration.

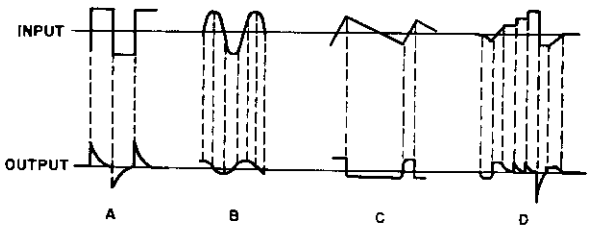


Differentiator Waveforms

With a square wave pulse of 100 volts amplitude applied as an input signal at time t_o, the output is a positive 100 volts spike. At this time there is no voltage drop across resistor R, since the inductive effect of L is to build up instantly a back emf that equals the applied signal and prevents instant current flow through the inductor. Between time t_o and t_1 current begins to flow through inductor L and a small voltage drop is developed across resistor R. As the current flow through R increases, the voltage drop (shown in dotted lines in the waveform figures) increases. Meanwhile, the voltage developed across the inductor, e_L,

is decreasing, and, since the output is taken across L, it is also decreasing (the decrease of voltage across coil L represents the voltage used in building up a magnetic field around L). The sum of the voltage drops across R and L equal the applied voltage. The current through inductor L increases exponentially and the voltage across resistor R increases, likewise. Since the time constant assumed in the illustration is 10 microseconds and the pulse width is 100 microseconds the steady-state condition is reached before the pulse ends. Since there now is no change in current, there is no voltage developed across the inductor and the output voltage is zero. At time t_1 the trailing edge of the input pulse occurs and drives the signal in a negative direction. Instantly a negative 100 volt spike appears across L and at the output. At the same time, the field around the coil collapses and produces a current through L in the opposite direction. During time t_1 to t_2 the negative voltage across the inductor decreases exponentially while the current increases exponentially. As the current flow through R increases, the voltage drop across it, likewise increases, and the sum of the voltage drops across R and L equals the applied voltage. With the 10 microsecond time constant and 100 microsecond pulse width, the steady state condition is again reached before the pulse ends. Since there now is no change in current, there is no voltage developed across the inductor and the output voltage is zero. At time t_2, the positive-going leading edge of the pulse appears and the cycle repeats.

The accompanying illustration shows the differentiated output waveforms for several different input wavef orms.



Differentiating Effects upon Different Waveforms

Although the circuit provides no amplification, for a square wave input, the peak output of the differentiator is twice that of the input signal. A positive pulse is produced for the positive leading edge and a negative pulse for the negative trailing edge.

With a sine-wave input the output remains a sine-wave as shown in part B of the illustration, the only differences being that the output sine-wave is of a smaller amplitude and is advanced in phase. The advance for a perfect differentiator is 90 degrees, but 89 degrees is not uncommon.

The sawtooth, shown in part C of the illustration is converted into a low amplitude square wave. Part D illustrates effect of a differentiator upon the application of a complex waveform.

Since the inductor has distributed (turns) capacitance across it, undesired resonant responses may occur in L-R circuits containing large values of inductance; therefore, the use of these networks is usually limited to high frequency applications.

FAILURE ANALYSIS.

No Output. Since only two components are involved, it is evident that only an open circuit at the input, or a short circuit at the output, could produce a no-output condition.

Low or Distorted Output. Only a change in component values or associated stray capacitance, inductance, and resistance values could change the time constant and waveshapes. Distorted output is usually caused by improper input signals. When checking the waveform at the differentiator, the effect of the shunt resistance or capacitance produced by the test instrument input should be considered. When distortion is discovered in the following tube circuits, it is probably caused by improper action in these circuits. A direct check of the output as compared with the input of the differentiator using a high-impedance oscilloscope, will indicate whether the circuit is performing properly. A shorted resistor or an open coil would cause the output to be a duplicate of the input (no differentiation taking place).

R-C INTEGRATOR.

APPLICATION.

The R-C integrator is used as a waveshaping network in radio, television, radar, and computers, as well as many other special electronic applications.

CHARACTERISTICS.

Input waveshape distorted (non-sinusoidal).
Produces a distortion of the input waveform.
Provides a wider range of time constants than an R-L integrator.
Has a long time constant.
Output is taken from across the capacitor.
Has the configuration of a low-pass filter.
No amplification is produced.

CIRCUIT ANALYSIS.

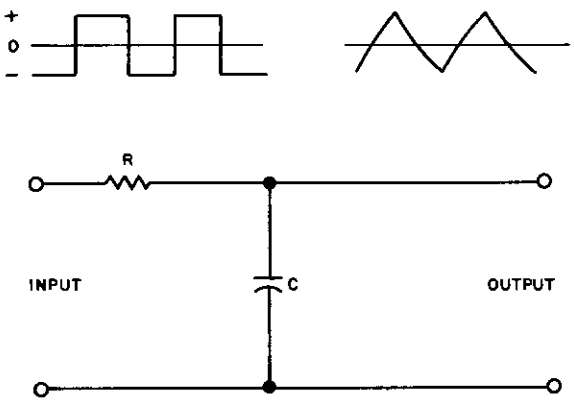
General. The R-C integrator circuit works in almost exact opposition to the R-C differentiator. It has a long time constant, and the output is taken from across the capacitor. The time constant of the integrator circuit should be 5 times (or more) the period of one alternation of the input waveform, for the circuit to electronically perform the mathematical operation of integration. As in the case of the differentiator, this action in practice is approximate, but the approximation can be made very close.

The higher the resistance in the R-C integrator, the more closely the output voltage follows the ideal integrator waveform. However, the higher this resistance, the smaller the output voltage. Conversely, decreasing the resistance in the R-C integrator circuit, results in a shorter time constant and a higher output voltage. However, as the resist-

ance is reduced in value, the output voltage departs from the ideal integrator waveform. In fact if the resistance, (and time constant) of the R-C circuit is sufficiently reduced, a point will be reached where the circuit no longer acts as an integrator.

The output of an integrator is in the form of a voltage that represents the average energy content of the input signal. For example, if the input is a steady d-c voltage, the same voltage will appear at the output, but, if the input is in the form of a series of narrow, widely separated pulses, the output voltage will be only a fraction of the input pulse value.

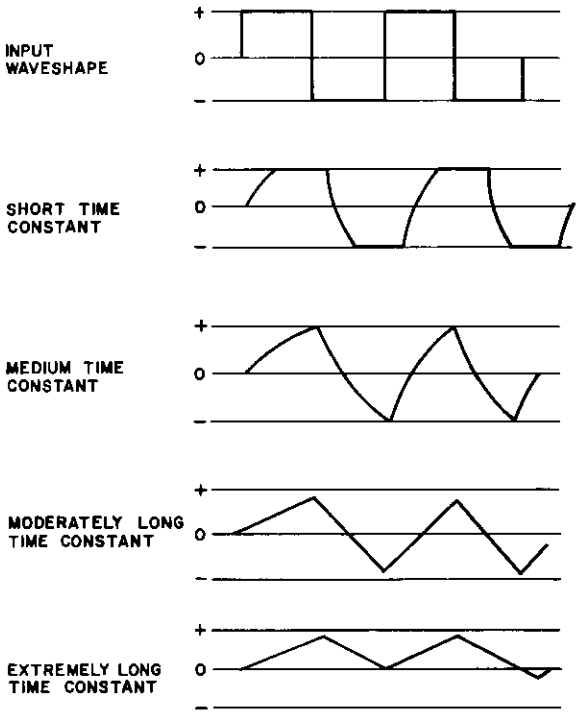
Circuit Operation. A schematic of a basic R-C integrator is shown in the accompanying illustration.



Basic R-C Integrator Circuit

As the square wave voltage applied to the input of the circuit goes positive, the capacitor charges exponentially at a rate determined by the time constant of the circuit. This time constant is calculated by multiplying the value of the resistor by the value of the capacitor (T=RC). For instance, a circuit containing a 100K resistor and a 50 picofarad capacitor would have a time constant of 5 microseconds, and if the value of the capacitor was increased ten times to 500 picofarads, the time constant would be ten times longer or 50 microseconds. The rise in voltage across the capacitor occurs as the voltage across R decreases from its maximum value. The voltage drop across the capacitor is always the difference between the input voltage and the voltage drop across the resistor. The rise in voltage across the capacitor occurs only for the duration of the applied square wave pulse. When the applied voltage drops from its maximum value, the capacitor discharges exponentially at the same rate that it charged, due to the time constant of the circuit. This gradual decrease in voltage across C effectively causes a negative pulse across R. If a square wave is applied to an R-C integrator circuit, a non-symmetrical saw-tooth waveform is produced. The principle of integration is used in saw-tooth generators to produce the linear rise in voltage by using a long time constant circuit, and to use only the straight portion of the exponential change waveform for linearity.

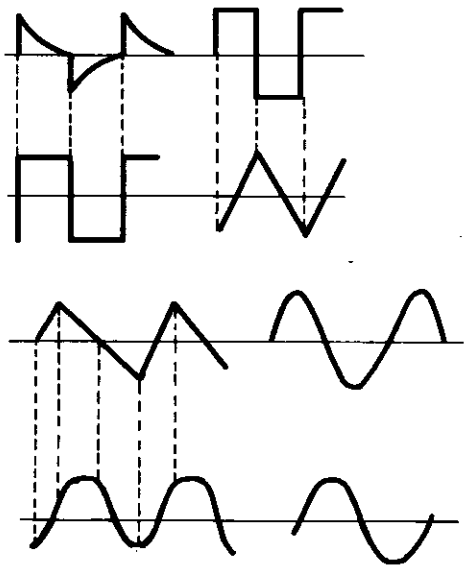
The accompanying waveform illustration shows the integrating effect of various time constants on a square wave.



Effects of Changing Time Constant

As can be seen from the waveforms in the illustration, a short time constant integrator does not change the input waveform very much except to distort the high frequency portions of the waveform (leading and trailing edges), and the low frequency (flat) portion is practically unchanged. As the time constant is changed to a medium value time constant, the waveshape changes to that of a rounded-off triangle (sweep waveform). With a moderately long time constant, the triangular waveform is equally distributed about the central zero axis and the sides are practically straight. When the time constant is made extremely long, it consists of somewhat elongated (stretched) sawtoothed waveforms of reduced amplitude which gradually approach the zero axis, and eventually, after a number of time constants, becomes symmetrically aligned around the center (zero) axis. A short time constant would be considered one which amounted to only one tenth of the pulse duration time. A medium time constant would be of the order of half the pulse duration, while a moderately long time constant would

be approximately equivalent to the full pulse width. A long or extremely long time constant would be considered to amount to two or three pulse widths or longer.



Integrating Effect of Different Waveforms

The accompanying illustration shows different types of inputs and their respective output for an R-C integrator circuit. The amplitudes of the waveshapes are different and bear no relotion to each other as shown in the illustration. When a peaked waveform is applied to an R-C integrator circuit, the resultant output will be a square waveform. Applying a square wave to the input of an integrator circuit produces an output waveform of trianqular shape. The integration of a triangular wave results in a parabolic output wave. Integrating a sine wave by an R-C circuit produces another sine wave with a different amplitude and phase, but with the same sinusoidal waveshape (usually considered to be a cosine waveform).

FAILURE ANALYSIS.

No Output. Since only two components are involved, it is evident that only an open circuit at the input, or a short circuit at the output, could produce a no-output condition (open resistor or shorted capacitor). Both of these items could be checked for with an ohmmeter. If the resistor is open the meter will indicate infinity, and if the capacitor is shorted the meter will read zero ohms.

Distorted Output. Only a change in component values, or associated component values, could change the time constant and waveshapes. Distorted output is usually caused by improper input signals. When distortion is discovered in the following tube or transistor circuits, it is probably caused by improper action in these circuits. A direct check of the output as compared with the input to the integrator using a high-impedance oscilloscope, will indicate whether the circuit is performing properly. A shorted resistor or an open capacitor would cause the output to be a duplicate of the input (no integration taking place). The value of the resistor can be checked with an ohmmeter. While the capacitor can also be checked for a short with the ohmmeter, it is better practice to use an in-circuit capacitance checker, and also to check the capacitor for both proper value and leakage.

R-L INTEGRATOR.

APPLICATION.

The R-L integrator is used as a waveshaping network in various types of electronic equipments such as radio, radar, television and in other special electronic application. It is also used as an analog in performing the mathematical function of integration in computers.

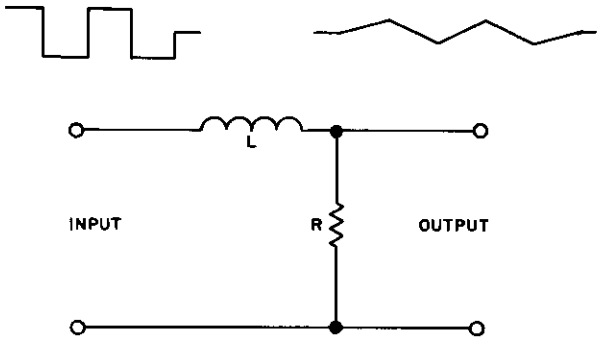
CHARACTERISTICS.

Produces distortion of the input waveshape.
Has a long time constant.
Output is taken across the resistor.
Has the configuration of a low pass filter.
Output is in the form of a voltage that represents the average energy content of the input waveform.

CIRCUIT ANALYSIS.

General. An integrating circuit is a circuit whose output is substantially the time integral of its input waveform. The R-L integrator circuit works in almost exact opposition to the R-L differentiator. It has a long time constant and the output is taken from across the resistor. If the time constant of the integrator circuit is 5 times (or more) the period of one alternation of the input waveform the circuit will electronically perform the mathematical operation of integration. This action is approximate in practice, but the approximation can be made very accurate. Since inductor action is the heart of the operation of the R-L integrator a brief review of inductor action follows. The property of inductonce is such as to oppose a change in current. This opposition (impedance) exerted by an inductor exists because a counter emf is produced across the inductor by the change in the magnetic field of the inductor. When a constant voltage is applied across an inductor, current flow does not rise to a maximum value immediately. Rather, it is initially zero and increases at an exponential rate, as the inductor becomes charged and the counter e.m.f. decreases. Likewise, when the applied voltage is removed, circuit current does not fall to zero immediately, but decreases at an exponential rate as the energy stored in the magnetic field of the inductor is discharged. In the R-L integrator circuit the longer the time constant, the more closely the output waveform follows the ideal integrator waveform. However, the longer the time constant, the smaller is the output voltage.

Circuit Operation. The accompanying schematic diagram illustrates a typical R-L integrator.

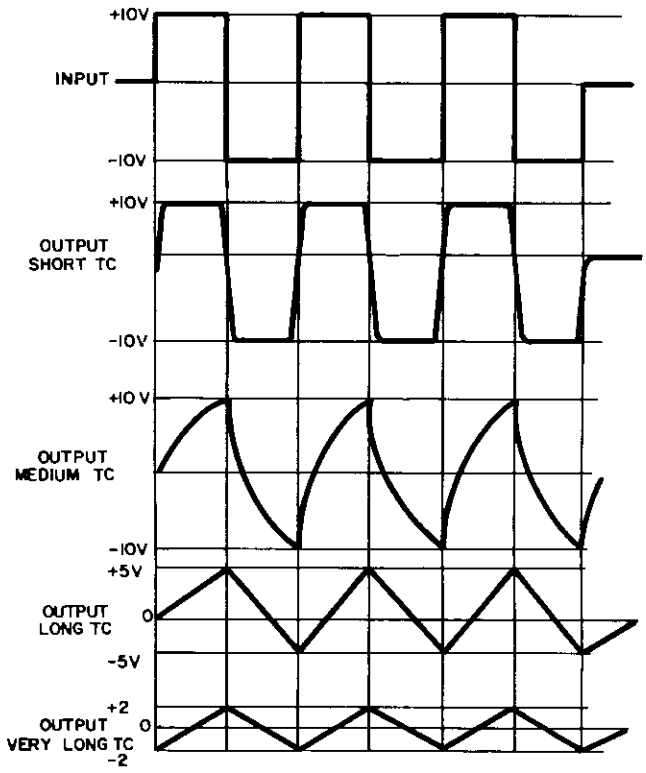


Typical R-L Integrator

This R-L integrator consists of a series R-L circuit with the output taken across the resistor. The charge and discharge time of the inductor (the time constant) is determined by the values of inductance and resistance in the circuit using the formula TC=L/R. Thus an integrator circuit consisting of a .1 henry inductor and a 10,000-ohm resistor has a time constant of 10 microseconds.

When a square wave is applied to the input of the integrator circuit the inductor begins to charge. The impedance, caused by counter e.m.f. generated by the expanding magnetic field is initially maximum, but decreases exponentially at a rate determined by the values of L and R as the magnetic field of the inductor approaches its limit. Circuit current, therefore, begins at zero and increases exponentially as the circuit impedance decreases. It is evident that the IR drop (voltage) across the output resistor begins at zero and increases as the inductor becomes charged. If the time constant is very long the increase in output voltage is nearly linear, but the peak of the output waveform attains only a fraction of the amplitude of the input signal, since the inductor attains only a slight charge during the period when voltage is applied to the input. When the input signal falls back to its reference level, the inductor discharges exponentially at the same rate as it charged. The decreasing current induced in the circuit by the collapsing field of the inductor results in a steadily decreasing voltage developed across output resistor R. The output of an integrator circuit with a long time constant (2 or more pulse widths), therefore, is a triangular waveform, which slopes up (positive) during the period when a positive pulse is applied, and slopes down (negative) during the period when the input is at its reference level. Conversely, when a negative going pulse is applied to the R-L integrator the output voltage goes negative and when the input voltage returns to its reference level the output voltage goes positive.

The following waveforms represent the integrating effects of various time constant integrator circuits on a square wave input.



Effects of Various Time Constants On A Square Wave

As can be seen from the waveforms in the illustration, a short time constant integrator has little effect on the output waveform, only the high frequency components (leading and trailing edges) are attenuated. As the time constant is increased the output begins to resemble a sweep waveform. A further increase in time constant results in a more linear rise and fall of the output waveform. Notice that the output waveform of the long and very long time constant integrator does not reach the peak amplitude of the input waveform, but is always a much lower value.

FAILURE ANALYSIS.

No Output. Since there are only two components in the R-L integrator, a no-output condition could only be caused by an open inductor, a shorted resistor, or by no signal input. Both the inductor and the resistor can easily be checked for the above mentioned conditions with an ohmmeter. Presence of the input signal can be determined by observing the waveform present at the input to the integrator with an oscilloscope.

Distorted Output. Generally speaking, an integrator circuit will either function as designed or not at all. However, it is possible for either the inductor or the resistor to change value. This would change the integrator time constant, and the output waveshape would be altered. The resistor may be checked for proper value with an ohmmeter, and the inductor can be checked for proper value with an impedance bridge. It is also possible for the inductor to become shorted or the resistor to become open. This would result in the output being a duplicate of the input (no integration taking place). The components can be checked as explained previously. The most common cause of distorted output is probably distorted input. The quality of the input signal can be easily determined by viewing the waveform present at the integrator input with an oscilloscope.

SATURABLE-CORE REACTOR PEAKING CIRCUIT.

APPLICATION.

The saturable-core reactor peaking circuit is used to produce a peaked pulse of voltage from a sine wave input.

CHARACTERISTICS.

Utilizes a saturable reactor.
Output voltage pulses are in phase with the input signal.
Usually operated near resonance.
Output pulse width is determined by the circuit Q.

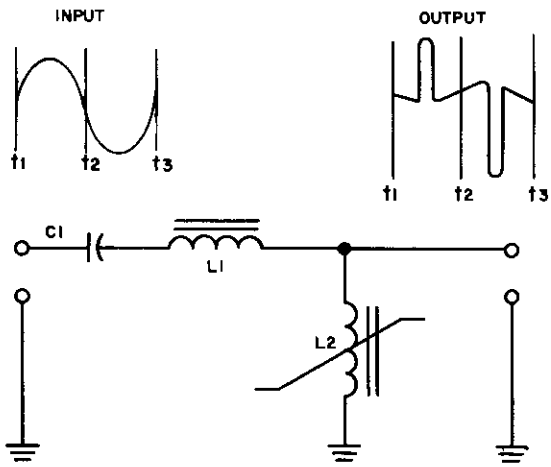
CIRCUIT ANALYSIS.

General. The saturable-core reactor peaking circuit produces sharp voltage pulses from a sine wave input signal by utilizing the properties of a saturable reactor. A saturable-core reactor is a type of inductor in which a relatively low value of current produces magnetic saturation of the core.

Magnetic saturation of an inductor core can be defined as the point where a further increase in current flow through the inductor windings does not result in any further increase in magnetic field. The property of inductance is such as to oppose a change in current. This opposition (impedance) exerted by an inductor exists because a counter e.m.f. is produced across the inductor, which opposes the applied voltage. If the core of a inductor were to become saturated, the counter e.m.f. would drop to a low value, and its opposition to current flow (impedance) would also drop to a low value. It is this ability to change impedance that enables the saturable-core reactor peaking circuit to produce a pulse output from a sinewave input.

Circuit Operation. The accompanying schematic diagram illustrates a typical saturable-core reactor peaking circuit.

The circuit illustrated above consists simply of conventional capacitor C1, conventional inductor L1, and saturable core reactor L2. Component values are chosen so that the circuit appears slightly capacitive when L2 is saturated and slightly inductive when L2 is unsaturated (the inductance of L2 decreases when L2 becomes saturated). To illustrate the capacitive-inductive relationships when L2



Saturable-Core Reactor Peaking Circuit

is saturated or unsaturated, assume for the sake of illustration that C1 has a capacitive reactance of 100 ohms at the operating frequency and that L1 has an inductive reactance of 75 ohms at the operating frequency. Assume further that L2 also has an inductive reactance of 40 ohms when unsaturated and 10 ohms when saturated. The reactance of both C1 and L1 remain constant. It can be seen that during the period when L2 is unsaturated there is a total of 115 ohms of inductive reactance and 100 ohms of capacitive reactance in the circuit. The circuit, therefore, appears inductive since the effect of L1 predominates. Likewise, when L2 is saturated there is 100 ohms of capacitive reactance but only 85 ohms of inductive reactance, and the circuit now appears capacitive.

When a sine wave is applied to the saturable-core reactor peaking circuit, L2 becomes saturated by the relatively high current flowing through it, and the voltage across L2 is very low, since the inductance of L2 is also very low at this time. Since the circuit is slightly capacitive during the saturation of L2, the current in the circuit leads the applied voltage by almost 90°, and the output voltage is approximately 180 degrees out of phase with the applied voltage, since the voltage across L2 also leads the current by nearly 90°. This output voltage is very low in amplitude, since L2 offers little impedance while in the saturated state. Inductor L2 becomes unsaturated when the input voltage is at a peak, since at this time circuit current is at a minimum due to the 90° phase shift. At this time (when L2 is unsaturated) the inductance of L2 becomes high. This makes the circuit highly inductive and causes the circuit current to lag the applied voltage by almost 90°. However, the voltage across L1 (the output) leads the circuit current by almost 90°, since voltage leads current across an induc-

tor and is, therefore, in phase with the input. This condition persists for only a short period of time until the circuit current increases and becomes sufficient to saturate L2. During this short period of time a large amplitude pulse which is inphase with the input is produced. The duration of this pulse coincides with the duration of the unsaturated condition of L2 and is determined mainly by the circuit Q. Thus, a large amplitude positive pulse is produced when the applied sine wave passes through its positive peak, and a large amplitude negative pulse is produced when the applied sine wave passes through its negative peak. Since L2 is saturated during most of the input cycle, the output is extremely low except for the short time during the peaks of voltage when L2 is in an unsaturated condition.

FAILURE ANALYSIS.

No Output. A no-output condition could result if any component in the saturable reactor peaking circuit became shorted or open. Inductors L1 and L2 can easily be checked by measuring the resistance of the windings and checking for a short or leakage to ground with an ohmmeter. Capacitor C1 can be checked with an in-circuit capacitor checker. Do not overlook the possibility that a no-output condition is the result of no-input. This can easily be checked by observing if the waveform is present at the circuit input with an oscilloscope.

Low Output. Generally speaking, since there are few components involved, the saturable-core reactor peaking circuit will either function as designed or not at all. However, a low-output condition could result from a partially shorted component or from excessive leakage to ground of the windings of L1 or L2, or from a low amplitude input. Resistance checks of the inductor windings and resistance checks to ground, with the bottom of L2 disconnected, should reveal whether or not a partially shorted component or leakage to ground is the cause of low output. The amplitude of the input signal can easily be checked by observing the waveform present at the input with an oscilloscope.

Distorted Output. Since the duration of the output pulse is determined mainly by the Q of the circuit, a change in circuit value could alter the Q of the circuit and thus alter the output waveshape. Checks for excessive leakage to ground should be made using an ohmmeter, since leakage to ground would affect the circuit Q. C1, L1 and L2 can be checked for proper value with an impedance bridge.

SEMICONDUCTOR PULSE SHAPER.

APPLICATION.

The semiconductor pulse shaper is used in computer, control, and communication equipment to reshape a pulse which has suffered deterioration of its waveshape after passing through a chain of gates. It is also used in conjunction with a multivibrator to form a 1 μ sec. pulse with sharp leading and trailing edges.

CHARACTERISTICS.

Reshapes pulses into pulses with sharp leading and trailing edges.

Utilizes two transistors connected in the common-emitter configuration.

Requires three power supply voltages.

Output pulse width is constant and is determined by circuit components.

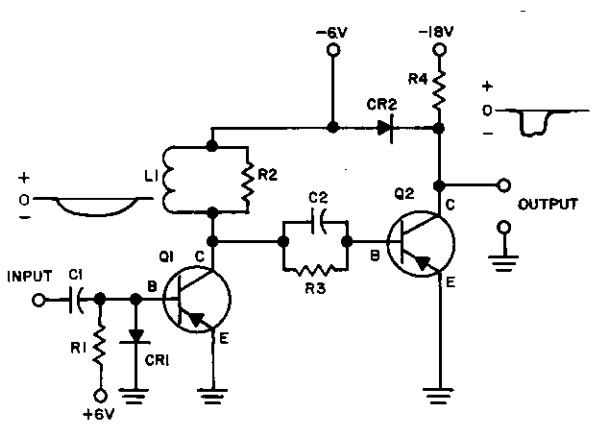
Capable of driving several loads.

CIRCUIT ANALYSIS.

General. The semiconductor pulse shaping circuit consists of two common-emitter amplifiers. The first stage, which employs an R-L collector load, performs the primary shaping function and controls the output pulse width. The second stage, an overdriven amplifier, serves as a buffer power amplifier, and in addition squares off the trailing edge of the output pulse.

The output pulse width is primarily determined by the values of the inductive load of the first stage and the input capacitor, but is also affected by transistor characteristics, as well as changes in the power supply voltage. In most instances circuit values are chosen which produce an output pulse width of 1 microsecond.

Circuit Operation. The accompanying schematic diagram illustrates a typical semiconductor pulse shaper using the common-emitter configuration.



Semiconductor Pulse Shaper

Capacitor C1 couples the input pulse to the base of transistor Q1. Resistor R1 and diode CR1 form a voltage divider between ground and the +6 volt bias supply to apply reverse bias to the base of transistor Q1. Inductor L1 and resistor R2 form the collector load for transistor Q1, and capacitor C2 together with resistor R3 forms an interstage coupling network from the collector of Q1 to the base of Q2. Transistor Q2, which is operated as an overdriven amplifier, serves as the output stage, with resistor R4 as its collector

load, and diode CR2 limiting the output to the level of the -6 volt power supply.

In the quiescent state (no signal input) transistor Q1 is reverse biased by the positive voltage at the junction of voltage divider R1-CR1. The collector of Q1 is at approximately -6 volts since Q1 forward collector current is cut off, and transistor Q2 is heavily forward biased by the negative collector voltage of Q1 direct-coupled through R3. With Q2 conducting heavily, the output voltage is very close to ground potential. When a negative pulse is applied to the pulse shaper, voltage divider diode CR1 is reverse biased and transistor Q1 is driven into conduction by the charging current flowing through the emitter-base junction of Q1 and into capacitor C1. The rapid rise in charging current through the emitter-base junction of Q1 rapidly drives Q1 into saturation, and the voltage on the collector of Q1 rises sharply to ground potential. This rapid positive swing in collector voltage on Q1 is coupled through R3 and C2 to the base of output transistor Q2, and Q2 is rapidly cutoff. The collector voltage of Q2 (the output voltage) which was previously held at ground potential due to the heavy conduction of Q2 now rapidly falls to the -6 volt supply level. This is the beginning of the output pulse. The amplitude of the output pulse is maintained at a constant -6 volts by the action of limiting diode CR2. Transistor Q1 is maintained in a saturated state by the charging current of C1 flowing through the emitter-base junction of Q1. This current decreases as C1 becomes charged, but remains sufficient to keep Q1 saturated for the duration of the output pulse. During the period when Q1 is saturated, collector current is limited by the impedance of the load (L1 and R2). Initially, the impedance of L1 is high, but it decreases as L1 becomes charged and collector current increases. Consequently, during the period when Q1 is in saturation, collector voltage on Q1 remains constant and output transistor Q2 remains cut off. Hence, the output voltage remains at -6 volts. When the desired output pulse width is completed, the impedance of L1 is so low that the base drive caused by the charging current of C1 is insufficient to maintain collector current at the previous level. (Base drive decreases as C1 charges). Collector current then decreases rapidly and Q1 collector voltage quickly falls to -6 volts, which drives output transistor Q2 into saturation. The output voltage rises sharply to ground potential as the conduction of Q2 increases. The rapid transition of Q2 from cutoff to saturation is aided by the discharge through the emitter-base junction of Q1, of the energy stored in L1. The term "cutoff" has been used loosely in the preceding paragraphs. Actually the transistors are not cut off in the sense that a vacuum tube can be cut off, since there is always some reverse leakage current flowing, but the magnitude of this current is insignificant. The values of C1 and L1 are the determining factors affecting output pulse width, since the output pulse is completed when C1 and L1 become fully charged and cause the collector current of Q1 to begin decreasing.

FAILURE ANALYSIS.

General. When making voltage checks, use a vacuum tube voltmeter to avoid the low values of multiplier resistance employed on the low voltage ranges of the standard 20,000 ohms-per-volt meter. Be careful also to observe proper polarity when checking continuity with an ohmmeter, since a forward bias through any of the transistor junctions will cause a false low resistance reading.

No Output. A no-output condition could result from failure of either transistor or failure of one of the power supplies. Semiconductor circuits are generally miniaturized printed circuits. Circuits of this type are subject to shorts caused by a small drop of solder, or any conductive object that may fall across printed circuit leads, or these leads may become open by a hairline crack in the printed board. Plug-in type contacts, often employed in printed circuit boards, sometimes fail to make contact due to dirty or bent contacts. It is often wise to visually check the printed circuit board for evidence of any of the above conditions before attempting to trouble-shoot the circuit. Power supply voltages should be checked with a vacuum-tube-voltmeter, and adjusted or repaired if necessary. It should be noted that deterioration with age causing lack of gain may result under high temperature conditions. Unlike vacuum tubes, however, transistors have operated for years without noticeable deterioration under proper operating conditions. If the transistor is not at fault, a defective circuit component is likely the cause of no output. Voltage checks of transistors elements with a vacuum tube voltmeter, or resistance checks with the circuit deenergized, should indicate the component at fault. Resistors R3 or R4 could cause a no-output condition if they failed, as could diode CR1 if it became shorted. Failure of other circuit components could possibly cause a no-output condition to exist, but are much more likely to cause distortion of the output waveshape. This condition will be discussed in detail in the following paragraph. Do no overlook the possibility that a no-output condition is the result of no input signal reaching the pulse shaper. The existance of this condition can readily be determined by observing the waveform present at the input to capacitor C1 with an oscilloscope.

Distorted Output. The term distorted output is used in the following paragraph to describe any output condition other than the proper output with respect to pulse width, pulse amplitude, and pulse rise and fall time since a circuit defect usually causes more than one of these symptoms of improper output to appear. Defective transistors and improper power supply voltages are often the cause of a distorted output. The power supply voltages should be checked and adjusted if necessary, they should be within 10% of their nominal values. If the power supply voltages are correct and the transistors are good, a defective circuit component is the next most likely cause of improper output. A significant change in the value of any component could alter the output waveshape. Since the value of L1 and C1 determine the pulse width a change in the value of these components would, naturally, affect the output pulse width. L1 and C1 can be checked for proper value on an inductance-capaci-

tance bridge. Resistors R1 and R2 also affect pulse width but to a lesser degree than C1 and L1. Diode CR2 limits the amplitude of the output pulse to –6 volts. If CR2 opened, the amplitude of the output pulse would increase. The input pulse must be of the correct polarity, and have sufficient amplitude and duration to properly trigger the pulse shaper, if a good output pulse is to be generated. The condition of the input pulse may be checked by observing the waveform present at the input to capacitor C1 with an oscilloscope.

SECTION 18

COUNTER CIRCUITS

PART A. ELECTRON-TUBE CIRCUITS

POSITIVE DIODE COUNTER.

APPLICATION.

The positive diode-counter circuit is supplied uniform input pulses, representing units to be counted, and produces a positive output voltage, the average value of which is proportional to the frequency of the applied pulses. Counter circuits are employed in the frequency-indicator circuits of electronic timing or counting devices.

CHARACTERISTICS.

Input pulses must be of constant amplitude and of equal time duration; a counter circuit must be preceded by limiting and shaping circuits to ensure uniform amplitude and width of input pulses.

Output-pulse polarity is positive; average d-c output voltage level is determined by input pulse-repetition frequency.

CIRCUIT ANALYSIS.

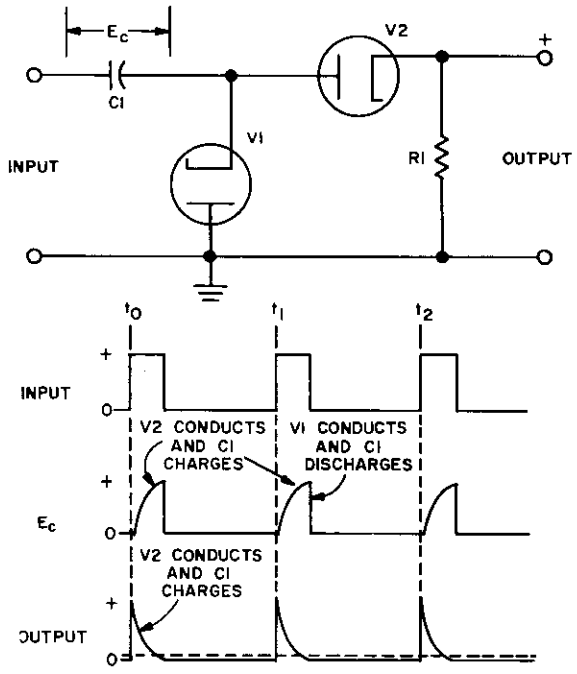
General. The positive counter circuit is used in frequency-indicator (timing or counting) circuits which depend upon the output pulse amplitude and time duration for accurate indications; therefore, the input pulses applied to the counter circuit must be of constant pulse amplitude and pulse width (time duration). The counter circuit is preceded by limiting and shaping circuits so that the only variable element in the counter-circuit output is the repetition frequency of the input signal, enabling input-frequency variations to be measured accurately. A relationship is thereby established between input frequency and average output voltage; as the input frequency increases the output voltage also increases and, conversely, as the input frequency decreases the output voltage decreases. Thus, the positive counter circuit, in effect, "counts" the number of positive-going input pulses and produces an average d-c output voltage which is proportional to the input repetition frequency.

The output of the positive counter circuit can also be used to produce positive trigger pulses to synchronize the frequency of blocking-oscillator or multivibrator circuits with the input pulse-repetition frequency. The basic positive counter circuit can be easily modified to change it to a step-by-step counter circuit (described later in this section) by substituting a capacitor for the resistor across the output terminals. This modified circuit is referred to as a **frequency divider**, because the output trigger frequency is usually made a submultiple of the input pulse-repetition frequency; the circuit is used in trigger-generator circuits of radar modulators and indicators.

Circuit Operation. A basic positive diode counter circuit is shown in the accompanying illustration, together with typical input and output waveforms. Capacitor C1 is the input coupling capacitor and also serves as a d-c blocking capacitor; resistor R1 is the load resistor across which the output voltage is developed. Electron tubes V1 and V2 are indirectly heated diodes; the filament (heater) circuit for the diodes is not shown on the schematic.

Initially, capacitor C1 assumes a charge (reference level) which is determined by the d-c voltage (if present) of the preceding stage. Once capacitor C1 is charged to the level of the applied d-c voltage, the circuit remains in a quiescent condition until an input is applied; the output voltage at this time is zero.

Pulses applied to the input of the counter circuit must have constant amplitude and equal time duration, since the counter circuit is intended to produce an output voltage which is proportional to the input pulse-repetition frequency. For the purpose of this discussion, assume that the input waveform shown in the accompanying illustration is applied to the input of the counter circuit.



Basic Positive-Diode Counter Circuit and Waveforms

When the positive-going leading edge of the input waveform occurs, the voltage rises suddenly. The charge on coupling capacitor C1 cannot change instantaneously; therefore, the plate of diode V2 becomes positive with respect to its cathode, and the diode conducts. Current flows through the series circuit consisting of load resistor R1 and diode V2 to charge the capacitor, C1. Since the charging current flows through the load resistor, R1, a pulse voltage is developed across the resistor and is supplied as the output of the counter circuit.

When the negative-going trailing edge of the input waveform occurs, the voltage drops suddenly. Once again the